PMC

Pm49FL002 / Pm49FL004

2 Mbit / 4 Mbit 3.3 Volt-only Firmware Hub/LPC Flash Memory

FEATURES

- **Single Power Supply Operation**
  - Low voltage range: 3.0 V - 3.6 V

- **Standard Intel Firmware Hub/LPC Interface**
  - Read compatible to Intel® 82802 Firmware Hub devices
  - Conforms to Intel LPC Interface Specification Revision 1.1

- **Memory Configuration**
  - Pm49FL002: 256K x 8 (2 Mbit)
  - Pm49FL004: 512K x 8 (4 Mbit)

- **Cost Effective Sector/Block Architecture**
  - Pm49FL002: Sixty-four uniform 4 Kbyte sectors, or sixteen uniform 16 Kbyte blocks (sector group)
  - Pm49FL004: One hundred and twenty-eight uniform 4 Kbyte sectors, or eight uniform 64 Kbyte blocks (sector group)

- **Top Boot Block**
  - Pm49FL002: 16 Kbyte top Boot Block
  - Pm49FL004: 64 Kbyte top Boot Block

- **Automatic Erase and Program Operation**
  - Build-in automatic program verification for extended product endurance
  - Typical 25 µs/byte programming time
  - Typical 50 ms sector/block/chip erase time

- **Two Configurable Interfaces**
  - In-System hardware interface: Auto detection of Firmware Hub (FWH) or Low Pin Count (LPC) memory cycle for in-system read and write operations
  - Address/Address-Multiplexed (A/A Mux) interface for programming on EPROM Programmers during manufacturing

- **Firmware HUB (FWH)/Low Pin Count (LPC) Mode**
  - 33 MHz synchronous operation with PCI bus
  - 5-signal communication interface for in-system read and write operations
  - Standard SDP Command Set
  - Data# Polling and Toggle Bit features
  - Register-based read and write protection for each block (FWH mode only)
  - 4 ID pins for multiple Flash chips selection (FWH mode only)
  - 5 GPI pins for General Purpose Input Register
  - TBL# pin for hardware write protection to Boot Block
  - WP# pin for hardware write protection to whole memory array except Boot Block

- **Address/Address Multiplexed (A/A Mux) Mode**
  - 11-pin multiplexed address and 8-pin data I/O interface
  - Supports fast programming on EPROM programmers
  - Standard SDP Command Set
  - Data# Polling and Toggle Bit features

- **Lower Power Consumption**
  - Typical 2 mA active read current
  - Typical 7 mA program/erase current

- **High Product Endurance**
  - Guarantee 100,000 program/erase cycles per single sector (preliminary)
  - Minimum 20 years data retention

- **Compatible Pin-out and Packaging**
  - 32-pin (8 mm x 14 mm) VSOP
  - 32-pin PLCC
  - Optional lead-free (Pb-free) package

- **Hardware Data Protection**

GENERAL DESCRIPTION

The Pm49FL002/004 are 2 Mbit/4 Mbit 3.3 Volt-only Flash Memories used as BIOS in PCs and Notebooks. These devices are designed to use a single low voltage, ranging from 3.0 Volt to 3.6 Volt, power supply to perform in-system or off-system read, erase and program operations. The 12.0 Volt V_{PP} power supply are not required for the program and erase operations of devices. The devices conform to Intel® Low Pin Count (LPC) Interface specification revision 1.1 and also read-compatible with Intel 82802 Firmware Hub (FWH) for most PC and Notebook applications. The Pm49FL002/004 support two configurable interfaces: In-system hardware interface which can automatic detect the FWH or LPC memory cycle for in-system read and write operations, and Address/Address Multiplexed (A/A Mux) interface for fast manufacturing on EPROM Programmers. These devices are designed to work with both Intel Family chipset and Non-Intel Family Chipset platforms, it will provide PC and Notebook manufacturers great flexibility and simplicity for design, procurement, and material inventory.

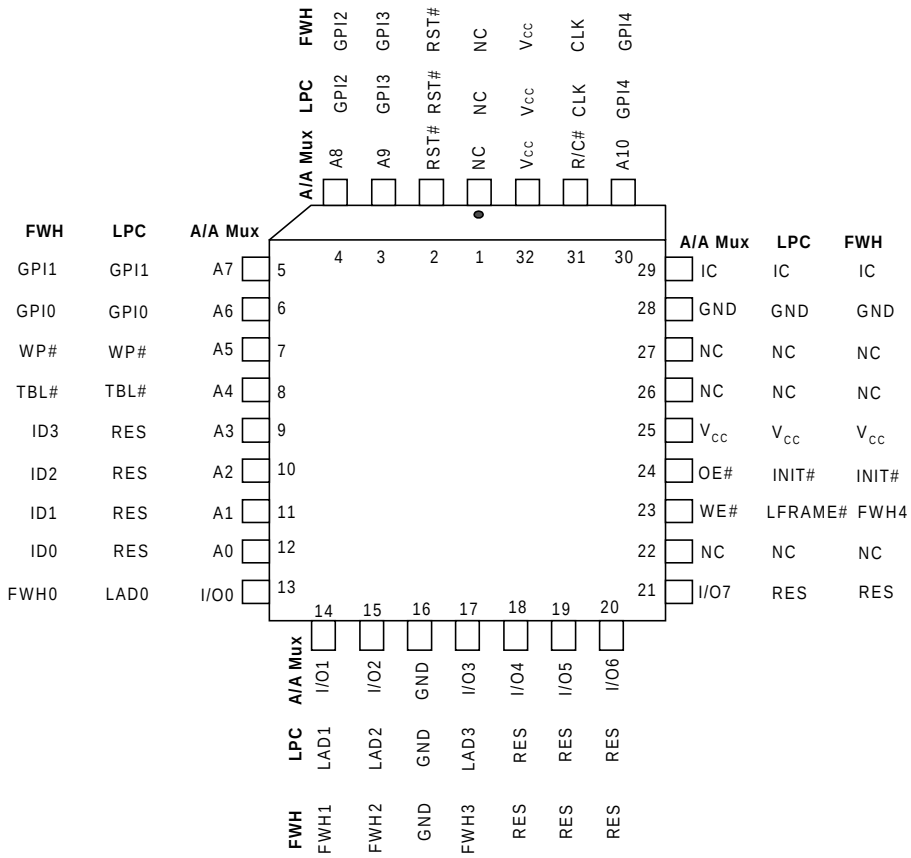
The memory array of Pm49FL002 is divided into uniform 4 Kbyte sectors, or uniform 16 Kbytes blocks (sector group - consists of four adjecent sectors). The memory array of Pm49FL004 is divided into uniform 4 Kbyte sectors, or uniform 64 Kbyte blocks (sector group - consists of sixteen adjecent sectors). The sector or block erase feature allows users to flexibly erase a memory area as small as 4 Kbyte or as large as 64 Kbyte by one single erase operation without affecting the data in others. The chip erase feature allows the whole memory to be erased in one single erase operation. The devices can be programmed on a byte-by-byte basis after performing the erase operation.

The program operation of Pm49FL002/004 is executed by issuing the program command code into command register. The internal control logic automatically handles the programming voltage ramp-up and timing. The erase operation of the devices is executed by issuing the sector, block, or chip erase command code into command register. The internal control logic automatically handles the erase voltage ramp-up and timing. The preprogramming on the array which has not been programmed is not required before an erase operation. The devices offer Data# Polling and Toggle Bit functions in FWH/LPC and A/A Mux modes, the progress or completion of program and erase operations can be detected by reading the Data# Polling on I/O7 or Toggle Bit on I/O6.

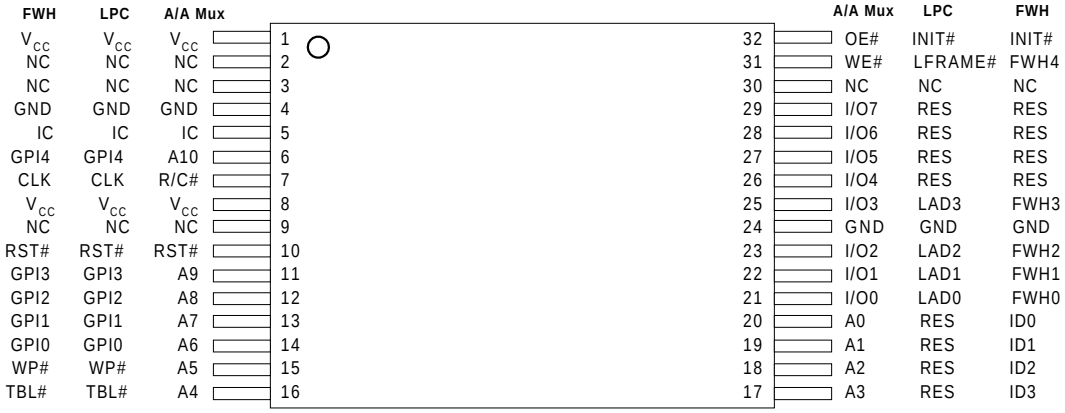
The Pm49FL002 has a 16 Kbyte top boot block which can be used to store user security data and code. The Pm49FL004 has a 64 Kbyte top boot block. The boot block can be write protected by a hardware method controlled by the TBL# pin or a register-based protection turned on/off by the Block Locking Registers (FWH mode only). The rest of blocks except boot block in the devices also can be write protected by WP# pin or Block Locking Registers (FWH mode only).

The Pm49FL002/004 are manufactured on PMC's advanced nonvolatile technology, P-FLASH™. The devices are offered in 32-pin VSOP and PLCC packages with optional environmental friendly lead-free package.

CONNECTION DIAGRAMS

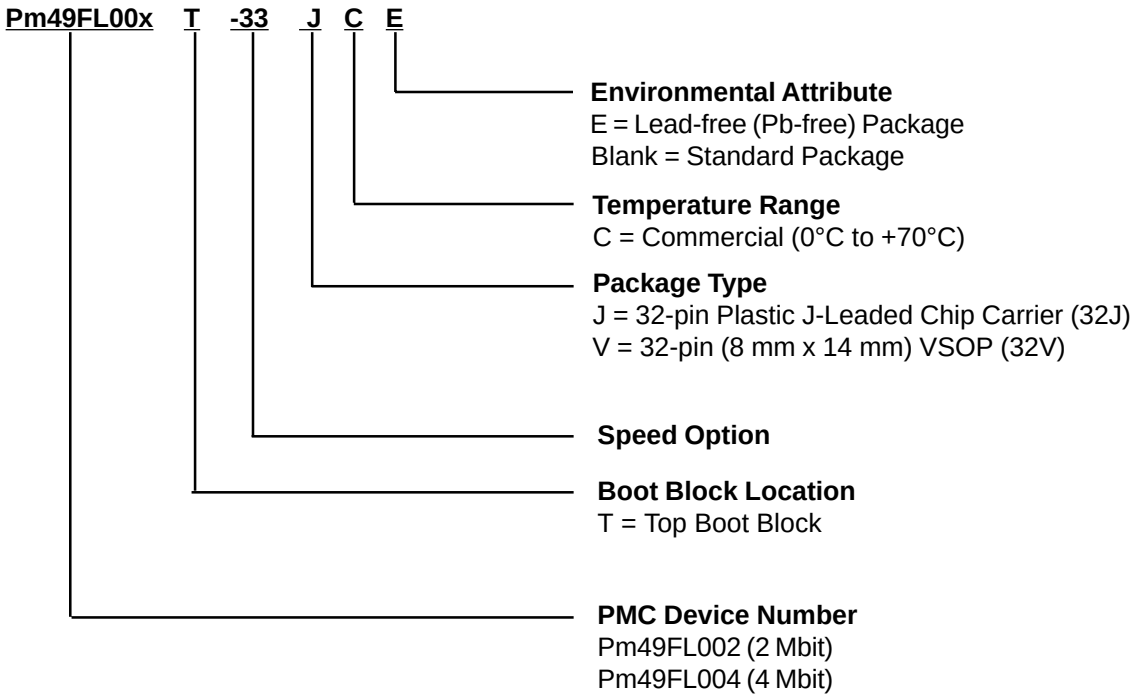


32-PIN PLCC



32-PIN (8mm x 14mm) VSOP

PRODUCT ORDERING INFORMATION



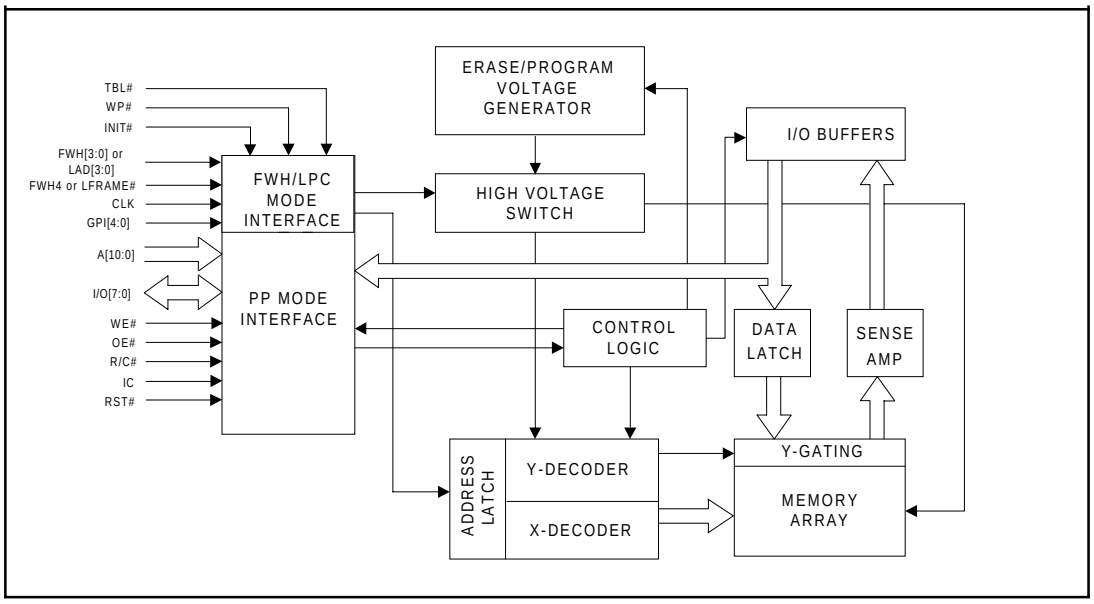
Part Number	MHz	Boot Block Location	Package	Temperature Range
Pm49FL002T-33JCE	33	Top	32J	Commercial (0°C to +70°C)
Pm49FL002T-33JC				
Pm49FL002T-33VCE			32V	
Pm49FL002T-33VC				
Pm49FL004T-33JCE	33	Top	32J	Commercial (0°C to +70°C)
Pm49FL004T-33JC				
Pm49FL004T-33VCE			32V	
Pm49FL004T-33VC				

PIN DESCRIPTIONS

SYMBOL	TYPE	Interface			DESCRIPTION
		PP	FWH	LPC	
A[10:0]	I	X			Address Inputs: For inputing the multiplex addresses and commands in PP mode. Row and column addresses are latched during a read or write cycle controlled by R/C# pin.
R/C#	I	X			Row/Column Select: To indicate the row or column address in PP mode. When this pin goes low, the row address is latched. When this pin goes high, the column address is latched.
I/O[7:0]	I/O	X			Data Inputs/Outputs: Used for A/A Mux mode only, to input command/data during write operation and to output data during read operation. The data pins float to tri-state when OE# is disabled.
WE#	I	X			Write Enable: Activate the device for write operation. WE# is active low.
OE#	I	X			Output Enable: Control the device's output buffers during a read cycle. OE# is active low.
IC	I	X	X	X	Interface Configuration Select: This pin determines which mode is selected. When pulls high, the device enters into A/A Mux mode. When pulls low, FWH/LPC mode is selected. This pin must be setup during power-up or system reset, and stays no change during operation. This pin is internally pulled down with a resistor between 20-100 KΩ.
RST#	I	X	X	X	Reset: To reset the operation of the device and return to standby mode.
INIT#	I		X	X	Initialize: This is a second reset pin for in-system use. INIT# or RST# pin pulls low will initiate a device reset.
GPI[4:0]	I		X	X	FWH/LPC General Purpose Inputs: Used to set the GPI_REG for system design purpose only. The value of GPI_REG can be read through FWH interface. These pins should be set at desired state before the start of the PCI clock cycle for read operation and should remain no change until the end of the read cycle. Unused GPI pins must not be floated.
TBL#	I		X	X	Top Block Lock: When pulls low, it enables the hardware write protection for top boot block. When pulls high, it disables the hardware write protection.
WP#	I		X	X	Write Protect: When pulls low, it enables the hardware write protection to the memory array except the top boot block. When pulls high, it disables hardware write protection.
FWH[3:0]	I/O		X		FWH Address and Data: The major I/O pins for transmitting data, addresses and command code in FWH mode.
FWH4	I		X		FWH Input: To indicate the start of a FWH memory cycle operation. Also used to abort a FHW memory cycle in progress.
LAD[3:0]	I/O			X	LPC Address and Data: The major I/O pins for transmitting data, addresses and command code in LPC mode.
LFRAME#	I			X	LPC Frame: To indicate the start of a LPC memory cycle operation. Also used to abort a LPC memory cycle in progress.
CLK	I		X	X	FWH/LPC Clock: To provide a synchronous clock for FWH and LPC mode operations.
ID[3:0]	I		X		Identification Inputs: These four pins are part of the mechanism that allows multiple FWH devices to be attached to the same bus. The strapping of these pins is used to identify the component. The boot device must have ID[3:0] = 0000b and it is recommended that all subsequent devices should use sequential up-count strapping. These pins are internally pulled-down with a resistor between 20-100 KΩ.
V_{CC}		X	X	X	Device Power Supply
GND		X	X	X	Ground
NC		X	X	X	No Connection
RES			X	X	Reserved: Reserved function pins for future use.

Note: I = Input, O = Output

BLOCK DIAGRAM



DEVICE OPERATION

MODE SELECTION

The Pm49FL002/004 can operate in two configurable interfaces: The In-System Hardware interface and Address/Address Multiplexed (A/A Mux) interface controlled by IC pin. If the IC pin is set to logic high (V_{IH}), the devices enter into A/A Mux interface mode. If the IC pin is set logic low (V_{IL}), the devices will be in in-system hardware interface mode. During the in-system hardware interface mode, the devices can automatically detect the Firmware Hub (FWH) or Low Pin Count (LPC) memory cycle sent from host system and response to the command accordingly. The IC pin must be setup during power-up or system reset, and stays no change during device operation.

When working in-system, typically on a PC or Notebook, the Pm49FL002/004 are connected to the host system through a 5-pin communication interface operated based on a 33-MHz synchronous clock. The 5-pin interface is defined as FWH[3:0] and FWH4 pins under FWH mode or as LAD[3:0] and LFRAME# pins under LPC mode for easy understanding as to those existing compatible products. When working off-system, typically on a EPROM Programmer, the devices are operated through 11-pin multiplexed address - A[10:0] and 8-pin data I/O - I/O[7:0] interfaces. The memory addresses of devices are input through two bus cycles as row and column addresses controlled by a R/C# pin.

PRODUCT IDENTIFICATION

The product identification mode can be used to read the Manufacturer ID and the Device ID by a software Product ID Entry command in both in-system hardware interface and A/A Mux interface modes. The product indentification mode is activated by three-bus-cycle command. Refer to Table 1 for the Manufacturer ID and Device ID of Pm49FL00x and Table 14 for the SDP Command Definition.

In FWH mode, the product identification can also be read directly at FFBC0000h for Manufacturer ID - “9Dh” and FFBC0001h for Device ID in the 4 GByte system memory map.

Table 1: Product Identification

Description		Address	Data
Manufacturer ID		00000h 00002h	9Dh 7Fh
Device ID Pm49FL002 Pm49FL004	 2Mb 4Mb	00001h	 6Dh 6Eh

DEVICE OPERATION (CONTINUED)

The Pm49FL002/004 provide three levels of data protection for the critical BIOS code of PC and Notebook. It includes memory hardware write protection, hardware data protection and software data protection.

MEMORY HARDWARE WRITE PROTECTION

The Pm49FL002 has a 16 Kbyte top boot block and the Pm49FL004 has a 64 Kbyte top boot block. When working in-system, the memory hardware write protection feature can be activated by two control pins - Top Block Lock (TBL#) and Write Protection (WP#) for both FWH and LPC modes. When TBL# is pulled low (V_{IL}), the boot block is hardware write protected. A sector erase, block erase, or byte program command attempts to erase or program the boot block will be ignored. When WP# is pulled low (V_{IL}), the Block 0 ~ Block 14 of Pm49FL002, or the Block 0 ~ Block 6 of Pm49FL004 (except the boot block) are hardware write protected. Any attemp to erase or program a sector or block within this area will be ignored.

Both TBL# and WP# pins must be set low (V_{IL}) for protection or high (V_{IH}) for un-protection prior to a program or erase operation. A logic level change on TBL# or WP# pin during a program or erase operation may cause unpredictable results.

The TBL# and WP# pins work in combination with the block locking registers. When active, these pins write protect the appropriate blocks regardless of the associated block locking registers setting.

HARDWARE DATA PROTECTION

Hardware data protection protects the devices from unintentional erase or program operation. It is performed by the devices automatically in the following three ways:
(a) V_{CC} Detection: if V_{CC} is below 1.8 V (typical), the program and erase functions are inhibited.
(b) Write Inhibit Mode: holding any of the signal OE# low, or WE# high inhibits a write cycle (A/A Mux mode only).
(c) Noise/Glitch Protection: pulses of less than 5 ns (typical) on the WE# input will not initiate a write cycle (A/A Mux mode only).

SOFTWARE DATA PROTECTION

The devices feature a software data protection function to protect the device from an unintentional erase or program operation. It is performed by JEDEC standard Software Data Protection (SDP) command sequences. See Table 14 for SDP Command Definition. A program operation is initiated by three memory write cycles of unlock command sequence. A chip (only available in A/A Mux mode), sector or block erase operation is initiated by six memory write cycles of unlock command sequence. During SDP command sequence, any invalid command or sequence will abort the operation and force the device back to standby mode.

BYTE PROGRAMMING

In program operation, the data is programmed into the devices (to a logical “0”) on a byte-by-byte basis. In FWH and LPC modes, a program operation is activated by writing the three-byte command sequence and program address/data through four consecutive memory write cycles. In A/A Mux mode, a program operation is activated by writing the three-byte command sequence and program address/data through four consecutive bus cycles. The row address (A10 - A0) is latched on the falling edge of R/C# and the column address (A21 - A11) is latched on the rising edge of R/C#. The data is latched on the rising edge of WE#. Once the program operation is started, the internal control logic automatically handles the internal programming voltages and timing.

A data “0” can not be programmed back to a “1”. Only erase operation can convert “0”s to “1”s. The Data# Polling on I/O7 or Toggle Bit on I/O6 can be used to detect when the programming operation is completed in FWH, LPC, and A/A Mux modes.

CHIP ERASE

The entire memory array can be erased by chip erase operation available under the A/A Mux mode operated by EPROM Programmer only. Pre-programs the device is not required prior to the chip erase operation. Chip erase starts immediately after a six-bus-cycle chip erase command sequence. All commands will be ignored once the chip erase operation has started. The Data# Polling on I/O7 or Toggle Bit on I/O6 can be used to detect the progress or completion of erase operation. The devices will return back to standy mode after the completion of chip erase.

DEVICE OPERATION (CONTINUED)

SECTOR AND BLOCK ERASE

The Pm49FL002 contains sixty-four uniform 4 Kbyte sectors, or sixteen uniform 16 Kbyte blocks (sector group - consists of four adjecent sectors). The Pm49FL004 contains one hundred and twenty-eight uniform 4 Kbyte sectors, or eight uniform 64 Kbyte blocks (sector group - consists of sixteen adjecent sectors). A sector erase command is used to erase an individual sector. A block erase command is used to erase an individual block. See Table 12 - 13 for Sector/Block Address Tables.

In FWH/LPC mode, an erase operation is activated by writing the six-byte command sequence through six consecutive write memory cycles. In A/A Mux mode, an erase operation is activated by writing the six-byte command in six consecutive bus cycles. Pre-programs the sector or block is not required prior to an erase operation.

I/O7 DATA# POLLING

The devices provide a Data# Polling feature to indicate the progress or the completion of a program or erase operation in all modes. During a program operation, an attempt to read the device will result in the complement of the last loaded data on I/O7. Once the program cycle is complete, the true data of the last loaded data is valid on all outputs. During an erase operation, an attempt to read the device will result a “0” on I/O7. After the erase cycle is complete, an attempt to read the device will result a “1” on I/O7.

I/O6 TOGGLE BIT

The Pm49FL002/004 also provide a Toggle Bit feature to detect the progress or the completion of a program or erase operation. During a program or erase operation, an attempt to read data from the devices will result in I/O6 toggling between “1” and “0”. When the program or erase operation is complete, I/O6 will stop toggling and valid data will be read. Toggle bit may be accessed at any time during a program or erase operation.

RESET

Any read, program, or erase operation to the devices can be reset by the INIT# or RST# pins. INIT# and RST# pins are internally hard-wired and have same function to the devices. The INIT# pin is only available in FWH and LPC modes. The RST# pin is available in all modes. It is required to drive INIT# or RST# pins low during system reset to ensure proper initialization.

During a memory read operation, pulls low the INIT# or RST# pin will reset the devices back to standby mode and then the FWH[3:0] of FWH interface or the LAD[3:0] of LPC interface will go to high impedance state. During a program or erase operation, pulls low the INIT# or RST# pin will abort the program or erase operation and reset the devices back to standby mode. A reset latency will occur before the devices resume to standby mode when such reset is performed. When a program or erase operation is reset before the completion of such operation, the memory contents of devices may become invalid due to an incomplete program or erase operation.

FWH MODE OPERATION

FWH MODE MEMORY READ/WRITE OPERATION

In FWH mode, the Pm49FL002/004 are connected through a 5-pin communication interface - FWH[3:0] and FWH4 pins to work with Intel® Family of I/O Controller Hubs (ICH) chipset platforms. The FWH mode also support JEDEC standard Software Data Protection (SDP) product ID entry, byte program, sector erase, and block erase command sequences. The chip erase command sequence is only available in A/A Mux mode.

The addresses and data are transmitted through the 4-bit FWH[3:0] bus synchronized with the input clock on CLK pin during a FWH memory cycle operation. The address or data on FWH[3:0] bus is latched on the rising edge of the clock. The pulse of FWH4 pin inserted for one clock indicates the start of a FWH memory read or memory write cycle.

Once the FWH memory cycle is started, asserted by FWH4, a START value "11xxb" is expected by Pm49FL002/004 as a valid command cycle and is used to indicates the type of memory cycle ("1101b" for FWH memory read cycle or "1110b" for FWH memory write cycle). Addresses and data are transferred to and from the device decided by a series of "fields". Field sequences and contents are strictly defined for FWH memory read and write operations. Refer to Table 2 and 3 for FWH Memory Read Cycle Definition and FWH Memory Write Cycle Definition.

There are 7 clock fields in a FWH memory cycle that gives a 28 bit memory address A27 - A0 through FWH[3:0] pins, but only the last five address fields will be decoded by the FWH devices. The Pm49FL002 decodes A17 - A0 with A19 and A18 ignored. The Pm49FL004 decodes A18 - A0 with A19 ignored. The address A22 has the special function of directing reads and writes to the Flash array when A22 = 1 or to the register space with A22 = 0. The A27 - A23 and A21 - A20 are don't care for the devices under FWH mode.

The Pm49FL002/004 are mapped within the top 4 Mbyte address range devoted to the FWH devices in the 4 Gbyte system memory space. Please see Table 11 for System Memory Map.

FWH ABORT OPERATION

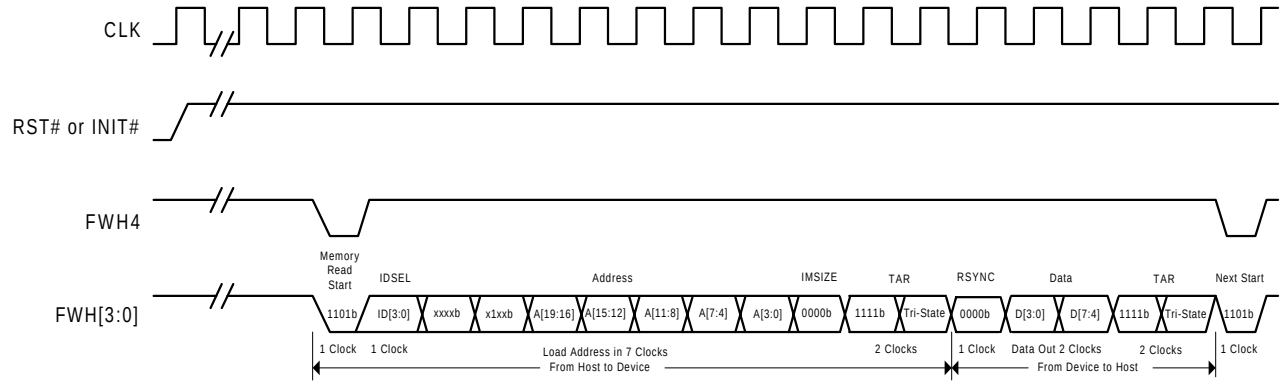
The FWH4 signal indicates the start of a memory cycle or the termination of a cycle in FWH mode. Asserting FWH4 for one or more clock cycle with a valid START value on FWH[3:0] will initiate a memory read or memory write cycle. If the FWH4 is driven low again for one or more clock cycles during this cycle, this cycle will be terminated and the device will wait for the ABORT command "1111b" to release the FWH[3:0] bus. If the abort occurs during the program or erase operation such as checking the operation status with Data# Polling (I/O7) or Toggle Bit (I/O6) pins, the read status cycle will be aborted but the internal program or erase operation will not be affected. Only the reset operation initiated by RST# or INIT# pin can terminate the program or erase operation.

FWH MODE OPERATION (CONTINUED)

Table 2: FWH Memory Read Cycle Definition

Clock Cycle	Field	FWH[3:0]	Direction	Description
1	START	1101	IN	Start of Cycle: "1101b" to indicate the start of a memory read cycle.
2	IDSEL	0000 to 1111	IN	ID Select Cycle: Indicates which FWH device should respond. If the IDSEL field matches the value set on ID[3:0] pins, then the particular FWH device will respond to subsequent commands.
3-9	IMADDR	YYYY	IN	Address Cycles: This is the 28-bit memory address. The addresses transfer most-significant nibble first and least-significant nibble last. (i.e., A27 - 24 on FWH[3:0] first, and A3 - A0 on FWH[3:0] last).
10	IMSIZE	0000	IN	Memory Size Cycle: Indicates how many bytes will be or transferred during multi-byte operations. The Pm49FL00x only support "0000b" for one byte operation.
11	TAR0	1111	IN then Float	Turn-Around Cycle 0: The Intel ICH has driven the bus then float it to all "1"s and then floats the bus.
12	TAR1	1111 (float)	Float then OUT	Turn-Around Cycle 1: The device takes control of the bus during this cycle.
13	RSYNC	0000 (READY)	OUT	Ready Sync: The FWH device indicates the least-significant nibble of data byte will be ready in next clock cycle.
14-15	DATA	YYYY	OUT	Data Cycles: The 8-bits data transferred with least-significant nibble first and most-significant nibble last. (i.e., I/O3 - I/O0 on LAD[3:0] first, then I/O7 - I/O4 on FWH[3:0] last).
16	TAR0	1111	OUT then Float	Turn -Around Cycle 0: The FWH device has driven the bus then float it to all "1"s and then floats the bus.
17	TAR1	1111 (float)	Float then IN	Turn-Around Cycle 1: The Intel ICH resumes control of the bus during this cycle.

FWH MEMORY READ CYCLE WAVEFORMS

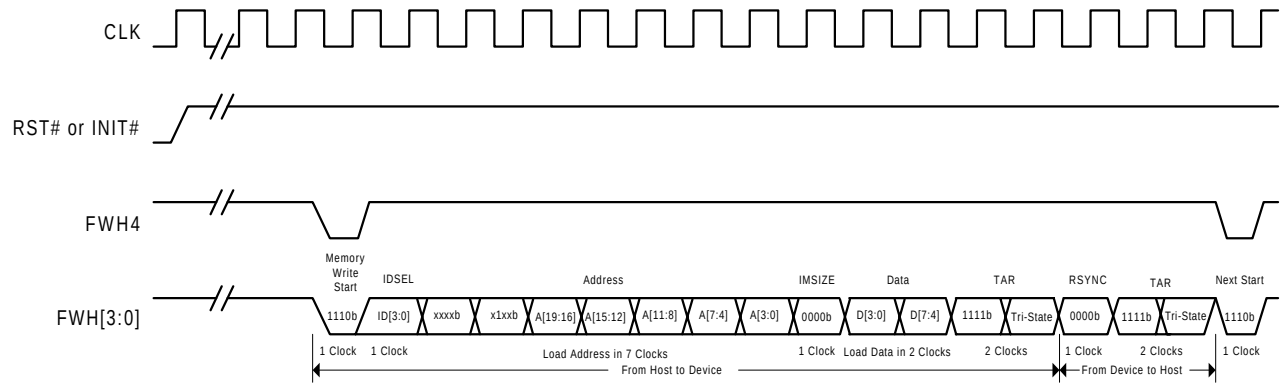


FWH MODE OPERATION (CONTINUED)

Table 3: FWH Memory Write Cycle Definition

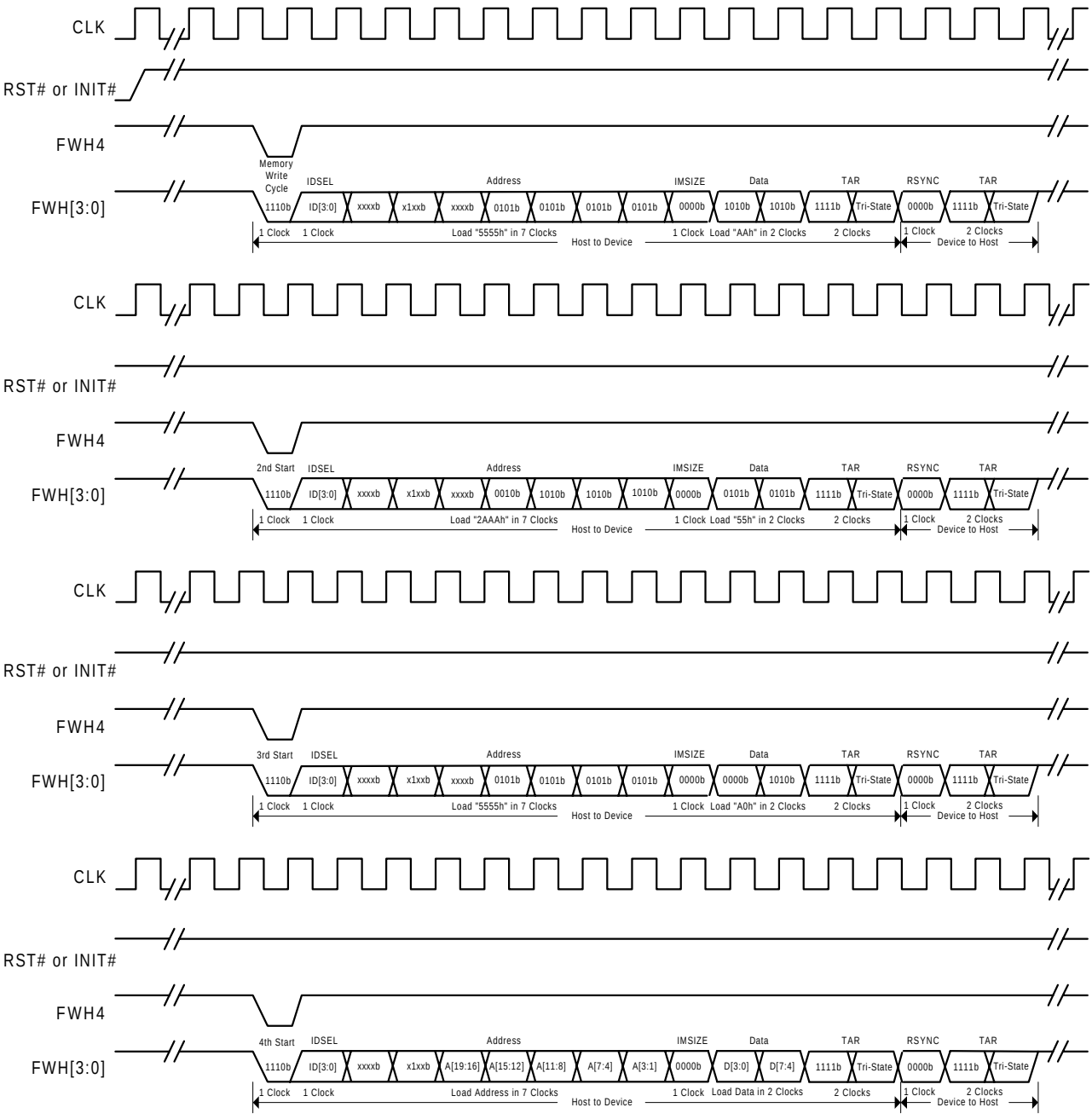
Clock Cycle	Field	FWH[3:0]	Direction	Description
1	START	1110	IN	Start of Cycle: "1110b" to indicate the start of a memory write cycle.
2	IDSEL	0000 to 1111	IN	ID Select Cycle: Indicates which FWH device should respond. If the IDSEL field matches the value set on ID[3:0] pins, then the particular FWH device will respond to subsequent commands.
3-9	IMADDR	YYYY	IN	Address Cycles: This is the 28-bit memory address. The addresses transfer most-significant nibble first and least-significant nibble last. (i.e., A27 - 24 on FWH[3:0] first, and A3 - A0 on FWH[3:0] last).
10	IMSIZE	0000	IN	Memory Size Cycle: Indicates how many bytes will be or transferred during multi-byte operations. The Pm49FL00x only support "0000b" for one byte operation.
11-12	DATA	YYYY	IN	Data Cycles: The 8-bits data transferred with least-significant nibble first and most-significant nibble last. (i.e., I/O3 - I/O0 on LAD[3:0] first, then I/O7 - I/O4 on FWH[3:0] last).
13	TAR0	1111	IN then Float	Turn-Around Cycle 0: The Intel ICH has driven the bus then float it to all "1"s and then floats the bus.
14	TAR1	1111 (float)	Float then OUT	Turn-Around Cycle 1: The device takes control of the bus during this cycle.
15	RSYNC	0000 (READY)	OUT	Ready Sync: The FWH device indicates that it has received the data or command.
16	TAR0	1111	OUT then Float	Turn-Around Cycle 0: The FWH device has driven the bus then float it to all "1"s and then floats the bus.
17	TAR1	1111 (float)	Float then IN	Turn-Around Cycle 1: The Intel ICH resumes control of the bus during this cycle.

FWH MEMORY WRITE CYCLE WAVEFORMS

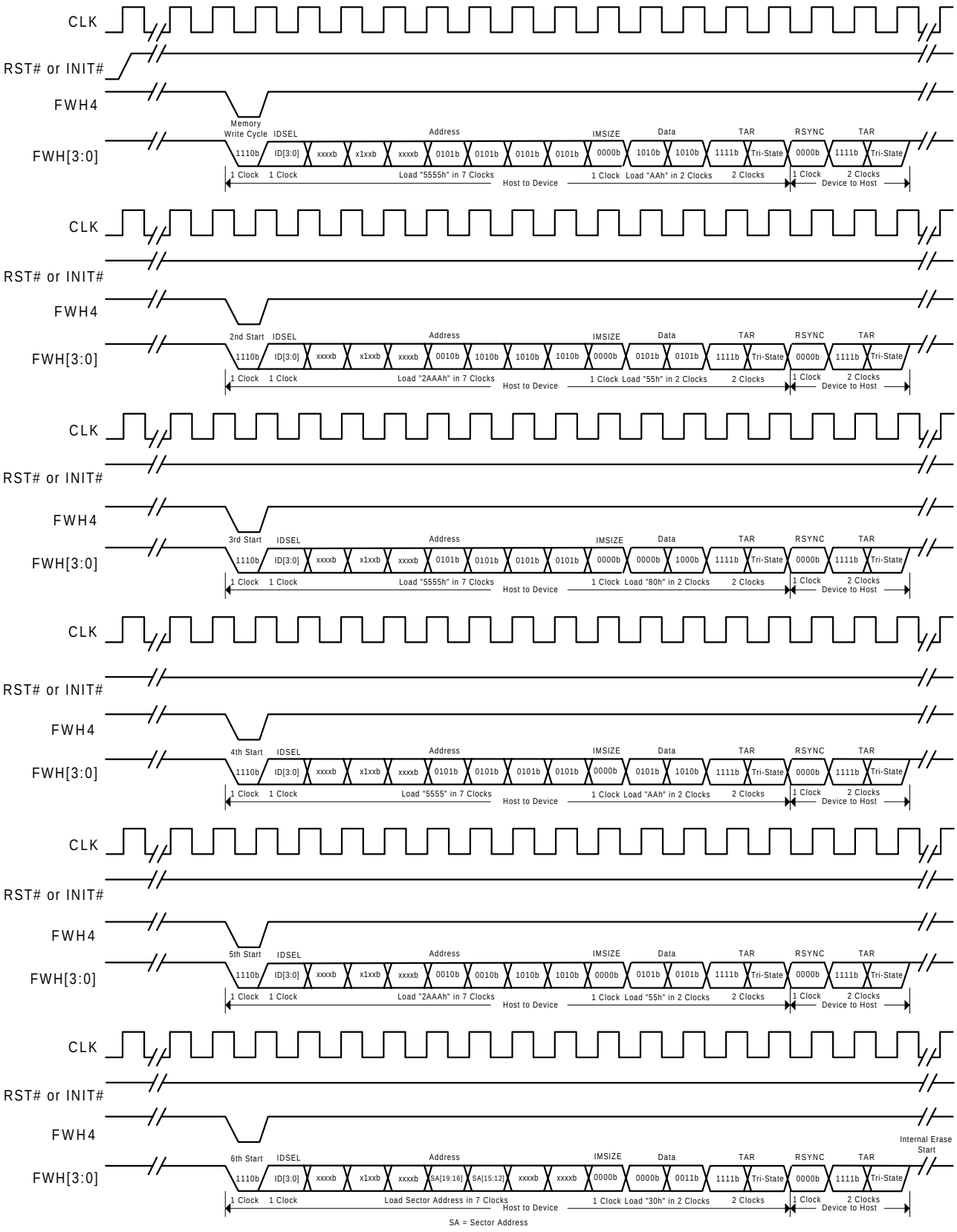


FWH MODE OPERATION (CONTINUED)

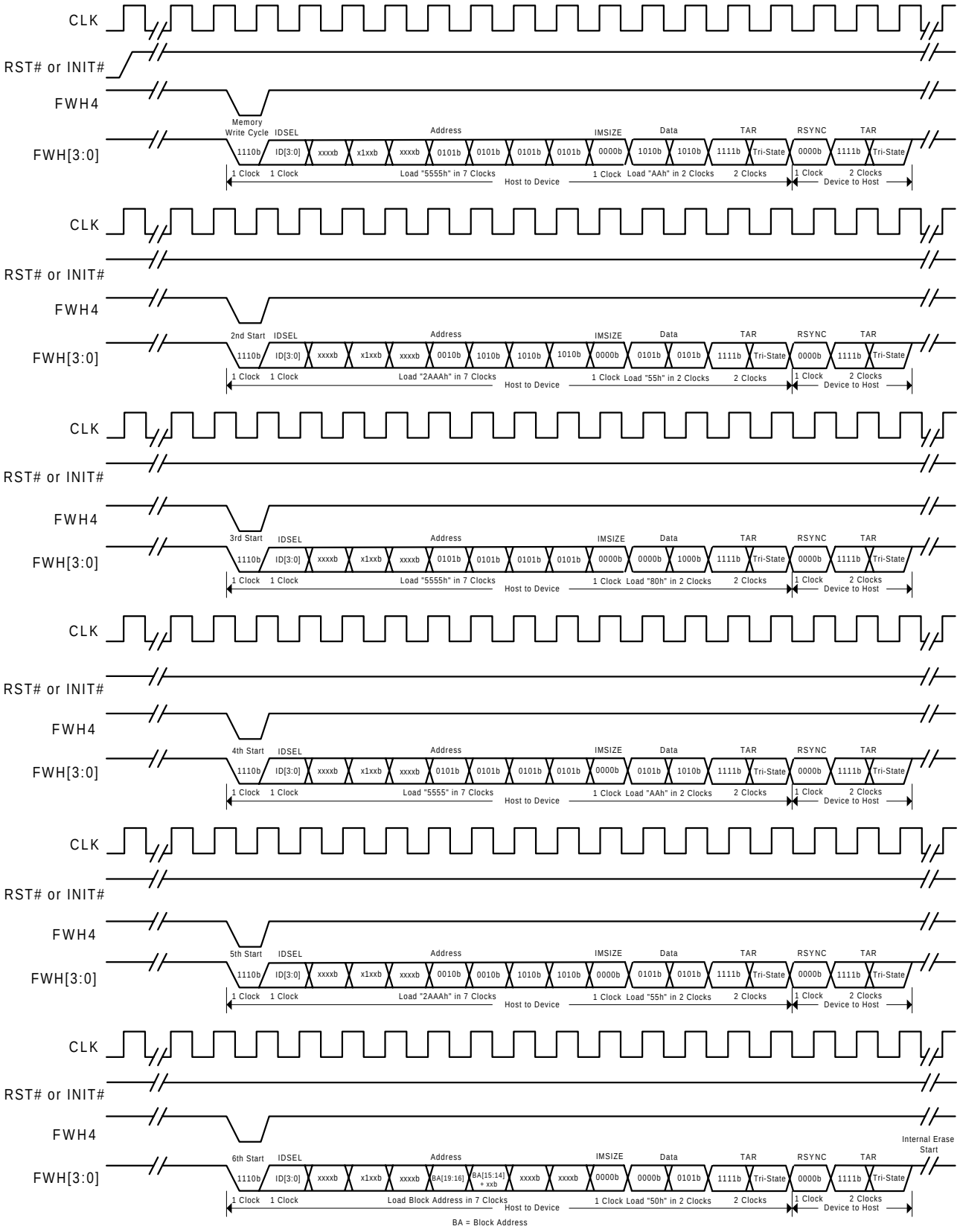
FWH BYTE PROGRAM WAVEFORMS



FWH SECTOR ERASE WAVEFORMS

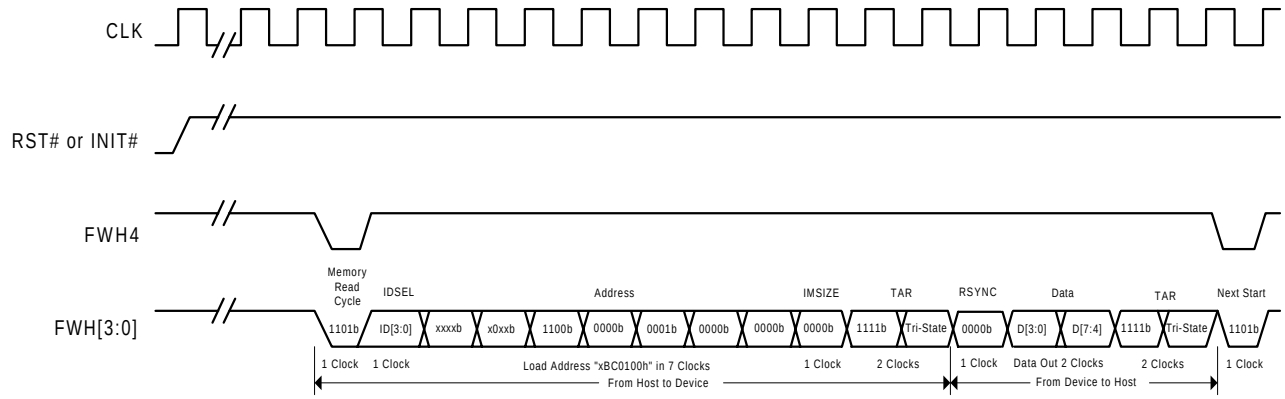


FWH BLOCK ERASE WAVEFORMS

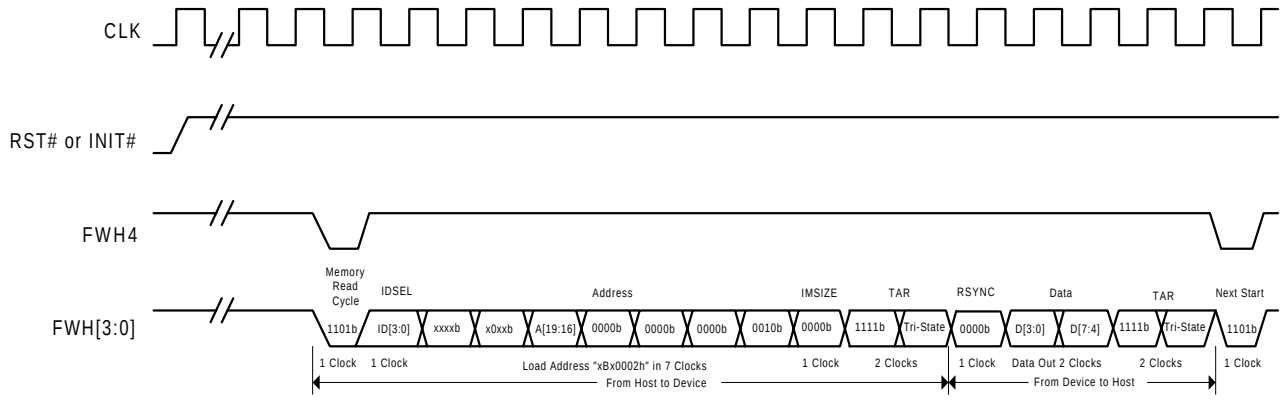


FWH MODE OPERATION (CONTINUED)

FWH GPI REGISTER READ WAVEFORMS



FWH BLOCK LOCKING REGISTER READ WAVEFORMS



LPC MODE OPERATION

LPC MODE MEMORY READ/WRITE OPERATION

In LPC mode, the Pm49FL002/004 use the 5-pin LPC interface includes 4-bit LAD[3:0] and LFRAME# pins to communicate with the host system. The addresses and data are transmitted through the 4-bit LAD[3:0] bus synchronized with the input clock on CLK pin during a LPC memory cycle operation. The address or data on LAD[3:0] bus is latched on the rising edge of the clock. The pulse of LFRAME# signal inserted for one or more clocks indicates the start of a LPC memory read or write cycle.

Once the LPC memory cycle is started, asserted by LFRAME#, a START value “0000b” is expected by the devices as a valid command cycle. Then a CYCTYPE + DIR value (“010xb” for memory read cycle or “011xb” for memory write cycle) is used to indicates the type of memory cycle. Refer to Table 4 and 5 for LPC Memory Read and Write Cycle Definition.

There are 8 clock fields in a LPC memory cycle that gives a 32 bit memory address A31 - A0 through LAD[3:0] with the most-significant nibble first. The memory space of Pm49FL002/004 are mapped directly to top of 4 Gbyte system memory space. See Table 11 for System Memory Map.

The Pm49FL002 is mapped to the address location of (FFFFFFFFh - FFFC0000h), the A31- A18 must be loaded with “1” to select and activate the device during a LPC memory read or write operation. Only A17 - A0 is used to decode and access the 256 Kbyte memory. The I/O7 - I/O0 data is loaded onto LAD[3:0] in 2 clock cycles with least-significant nibble first and most-significant nibble last.

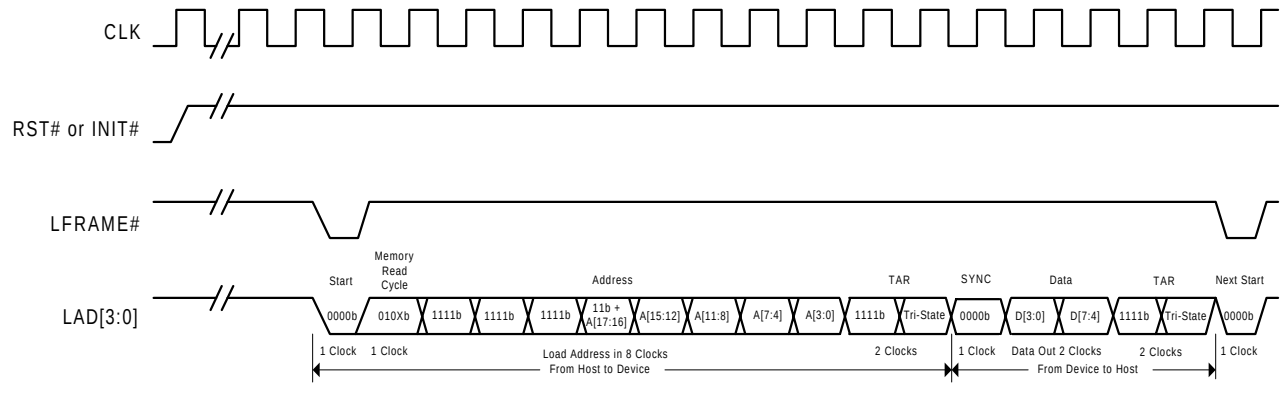
The Pm49FL004 is mapped to the address location of (FFFFFFFFh - FFF80000h), the A31- A19 must be loaded with “1” to select and activate the device during a LPC memory operation. Only A18 - A0 is used to decode and access the 512 Kbyte memory.

LPC MODE OPERATION (CONTINUED)

Table 4: LPC Memory Read Cycle Definition

Clock Cycle	Field	LAD[3:0]	Direction	Description
1	START	0000	IN	Start of Cycle: "0000b" indicates the start of a LPC memory cycle.
2	CYCTYPE + DIR	010x	IN	Cycle Type: Indicates the type of a LPC memory read cycle. CYCTYPE: Bits 3 - 2 must be "01b" for memory cycle. DIR: Bit 1 = "0b" indicates the type of cycle for Read. Bit 0 is reserved.
3 - 10	ADDR	YYYY	IN	Address Cycles: This is the 32-bit memory address. The addresses transfer most-significant nibble first and least-significant nibble last. (i.e., A31 - 28 on LAD[3:0] first, and A3 - A0 on LAD[3:0] last).
11	TAR0	1111	IN then Float	Turn-Around Cycle 0: The Chipset has driven the bus to all "1"s and then float the bus.
12	TAR1	1111 (float)	Float then OUT	Turn-Around Cycle 1: The device takes control of the bus during this cycle.
13	SYNC	0000	OUT	Sync: The device indicates the least-significant nibble of data byte will be ready in next clock cycle.
14 - 15	DATA	YYYY	OUT	Data Cycles: The 8-bits data transferred with least-significant nibble first and most-significant nibble last. (i.e., I/O3 - I/O0 on LAD[3:0] first, then I/O7 - I/O4 on LAD[3:0] last).
16	TAR0	1111	OUT then Float	Turn-Around Cycle 0: The device has driven the bus to all "1"s and then floats the bus.
17	TAR1	1111 (float)	Float then IN	Turn-Around Cycle 1: The Chipset resumes control of the bus during this cycle.

LPC MEMORY READ CYCLE WAVEFORMS

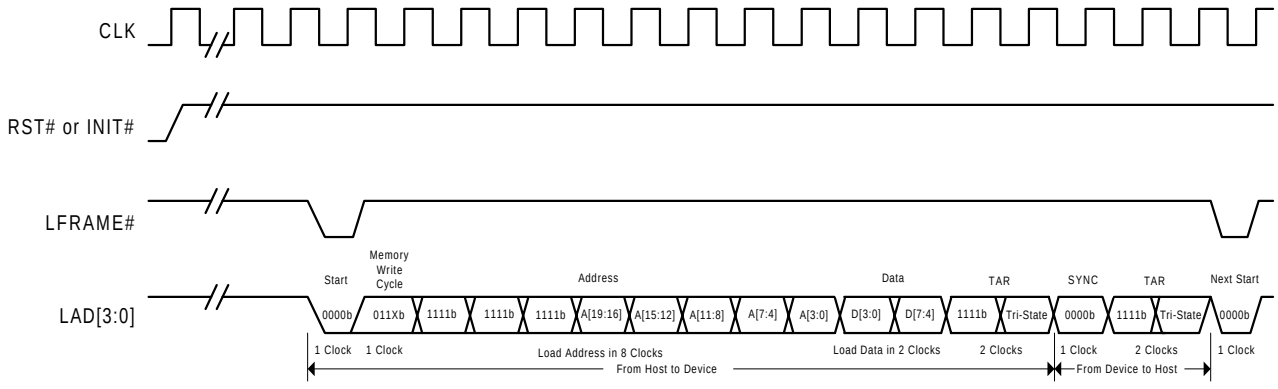


LPC MODE OPERATION (CONTINUED)

Table 5: LPC Memory Write Cycle Definition

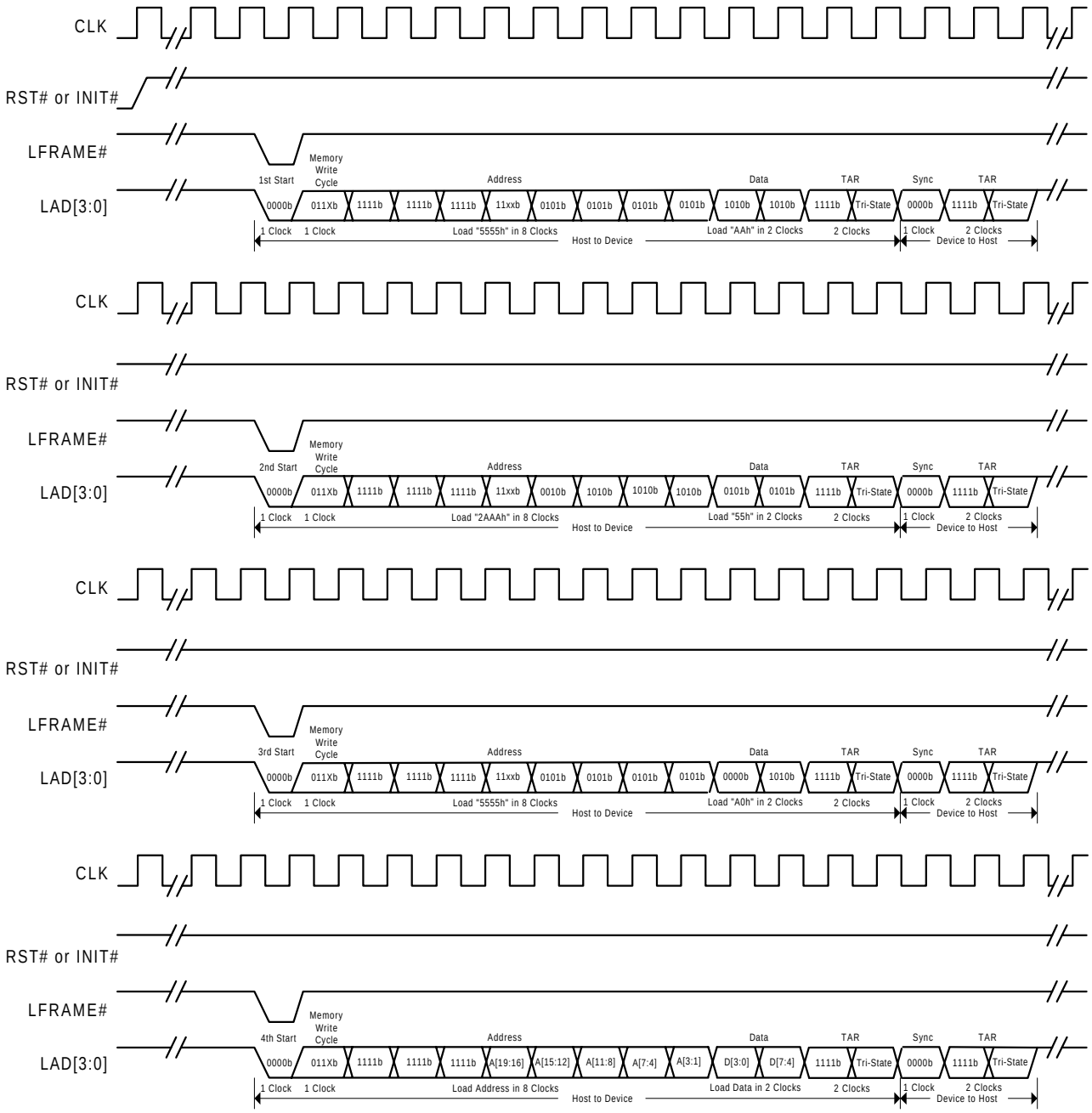
Clock Cycle	Field	LAD[3:0]	Direction	Description
1	START	0000	IN	Start of Cycle: "0000b" to indicate the start of a LPC memory cycle.
2	CYCTYPE + DIR	011x	IN	Cycle Type: Indicates the type of a LPC memory write cycle. CYCTYPE: Bits 3 - 2 must be "01b" for memory cycle. DIR: Bit 1 = "1b" indicates the type of cycle for Write. Bit 0 is reserved.
3 - 10	ADDR	YYYY	IN	Address Cycles: This is the 32-bit memory address. The addresses transfer most-significant nibble first and least-significant nibble last. (i.e., A31 - 28 on LAD[3:0] first, and A3 - A0 on LAD[3:0] last).
11 - 12	DATA	YYYY	IN	Data Cycles: The 8-bits data transferred with least-significant nibble first and most-significant nibble last. (i.e., I/O3 - I/O0 on LAD[3:0] first, then I/O7 - I/O4 on LAD[3:0] last).
13	TAR0	1111	IN then Float	Turn-Around Cycle 0: The Chipset has driven the bus to all "1"s and then float the bus.
14	TAR1	1111 (float)	Float then OUT	Turn-Around Cycle 1: The device takes control of the bus during this cycle.
15	SYNC	0000	OUT	Sync: The device indicates that it has received the data or command.
16	TAR0	1111	OUT then Float	Turn-Around Cycle 0: The device has driven the bus to all "1"s and then floats the bus.
17	TAR1	1111 (float)	Float then IN	Turn-Around Cycle 1: The Chipset resumes control of the bus during this cycle.

LPC MEMORY WRITE CYCLE WAVEFORMS

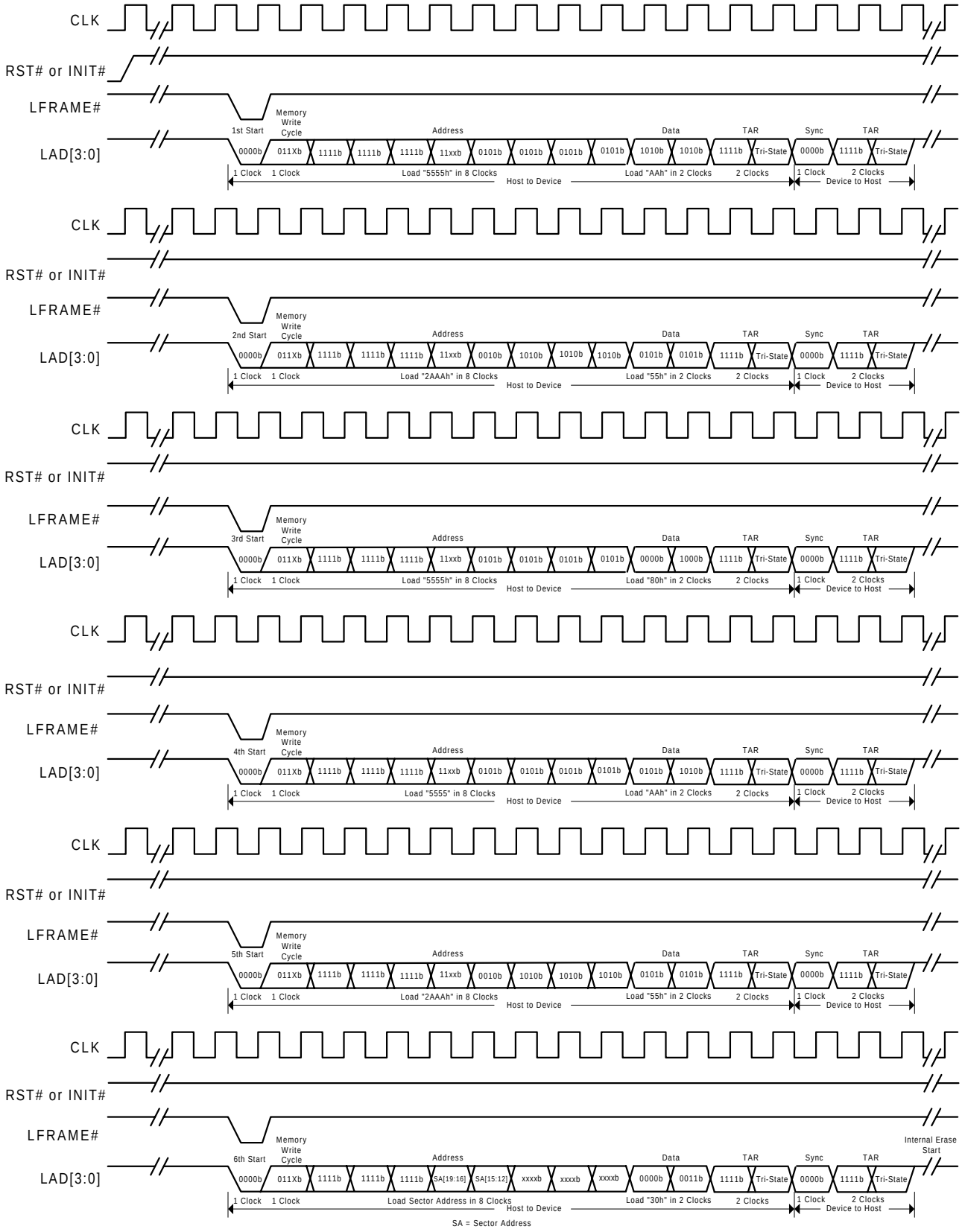


LPC MODE OPERATION (CONTINUED)

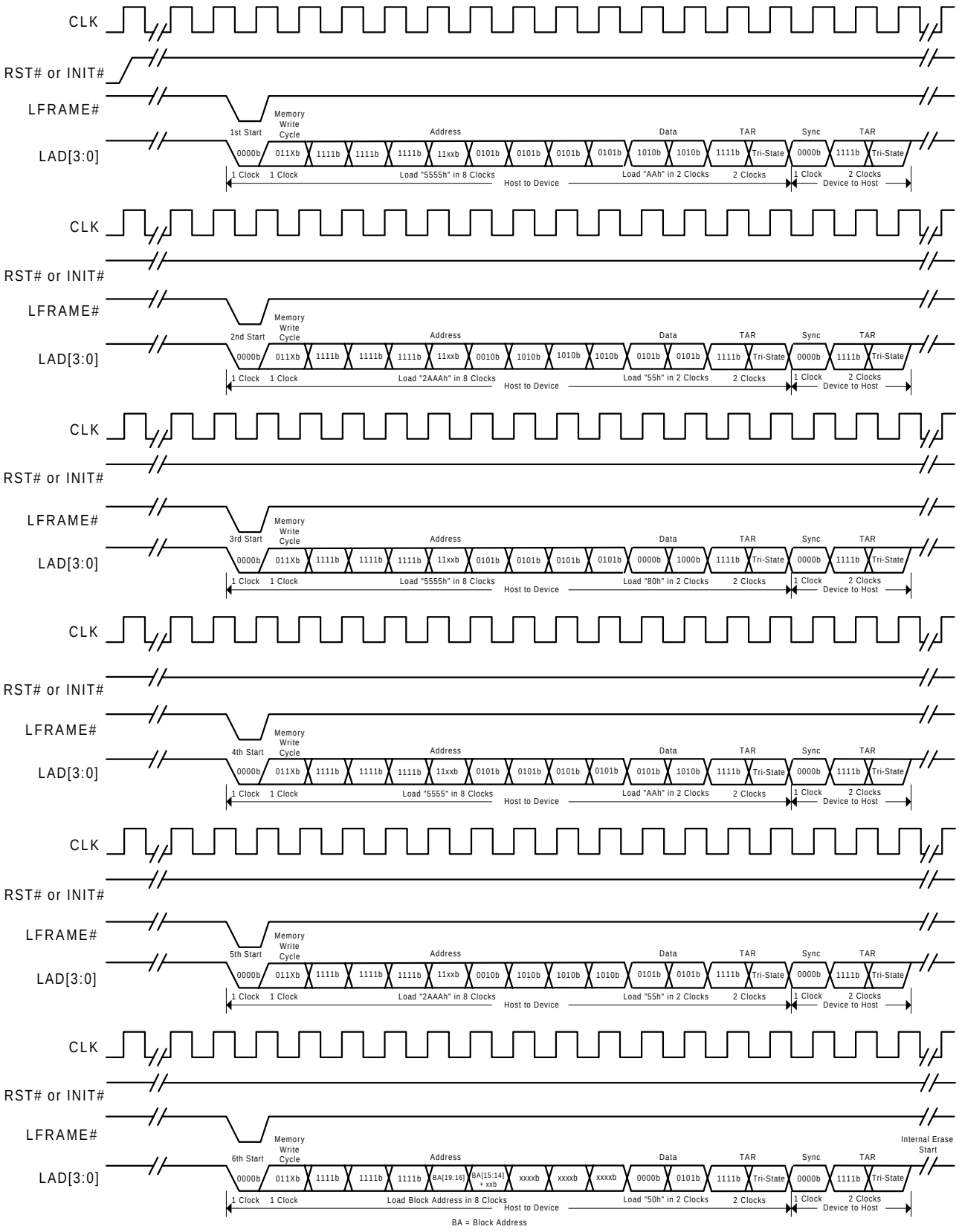
LPC BYTE PROGRAM WAVEFORMS



LPC SECTOR ERASE WAVEFORMS

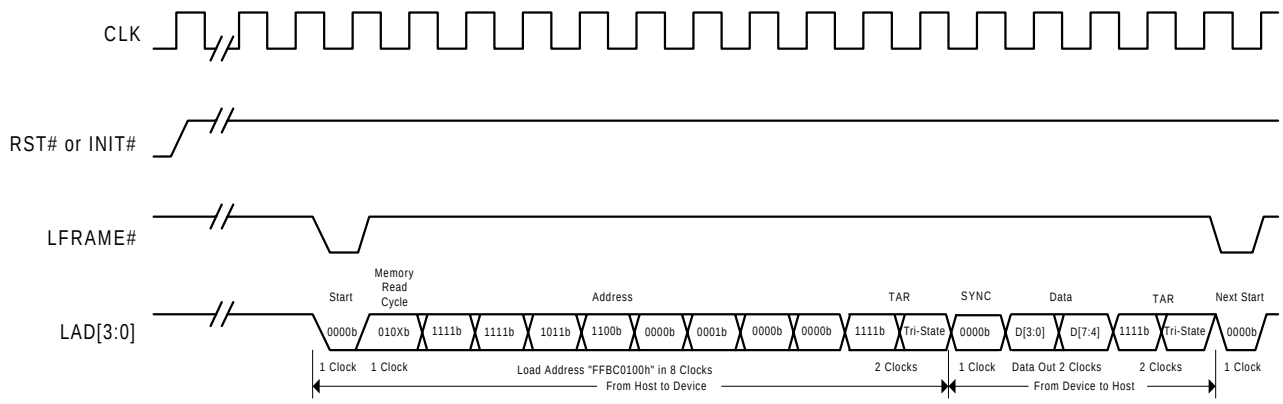


LPC BLOCK ERASE WAVEFORMS



LPC MODE OPERATION (CONTINUED)

LPC GPI REGISTER READ WAVEFORMS



REGISTERS

The Pm49FL002/004 have two registers include the General Purpose Inputs Register (GPI_REG - available in FWH and LPC modes) and the Block Locking Register (BL_REG - available in FWH mode only). The GPI_REG can be read at FFBC0100h in the 4 Gbyte system memory map. And the BL_REG can be read through FFBx0002h where x = F - 0h. See Table 8 and 9 for the address of BL_REG.

GENERAL PURPOSE INPUTS REGISTER

The Pm49FL002/004 contain an 8-bit General Purpose Inputs Register (GPI_REG) available in FWH and LPC modes. Only Bit 4 to Bit 0 are used in current version and Bit 7 to Bit 5 are reserved for future use. The GPI_REG is a pass-through register with the value set by GPI[4:0] pin during power-up. The GPI_REG is used for system design purpose only, the devices do not use this register. This register is read only and can be read at address location FFBC0100h in the 4 GByte system memory map through a memory read cycle. Refer to Table 6 for General Purpose Input Register Definition.

BLOCK LOCKING REGISTERS

The devices support block read-lock, write-lock, and lock-down features through a set of Block Locking Registers. Each memory block has an associated 8-bit read/writable block locking register. Only Bit 2 to Bit 0 are used in current version and Bit 7 to Bit 3 are reserved for future use. The default value of BL_REG is “01h” at power up. The definition of BL_REG is listed in Table 7. The FWH Register Configuration Map of Pm49FL002 is shown in Table 8. The FWH Register Configuration Map of Pm49FL004 is shown in Table 9. Unused register will be read as 00h.

Table 6. General Purpose Inputs Register Definition

Bit	Bit Name	Function	32-PLCC Pin#	32-VSOP Pin#
7:5		Reserved	-	-
4	GPI4	GPI_REG Bit 4	30	6
3	GPI3	GPI_REG Bit 3	3	11
2	GPI2	GPI_REG Bit 2	4	12
1	GPI1	GPI_REG Bit 1	5	13
0	GPI0	GPI_REG Bit 0	6	14

REGISTERS (CONTINUED)

Table 7. Block Locking Register Definition

Bit	Function
7:3	**Reserved**
2	**Read-Lock** "1" = Prevents read operations in the block where set. "0" = Normal operation for reads in the block where clear. Default state.
1	**Lock-Down** "1" = Prevents further set or clear operations to the Write-Lock and Read-Lock bits. Lock-Down only can be set, but not cleared. The block will remain locked-down until reset (with RST# or INIT#), or until the device is power-on reset. "0" = Normal operation for Write-Lock and Read-Lock bit altering in the block where clear. Default state.
0	**Write-Lock** "1" = Prevents program or erase operations in the block where set. Default state. "0" = Normal operation for programming and erase in the block where clear.

Data	Bit[7:3]	Bit 2	Bit 1	Bit 0	Resulting Block State
00h	00000	0	0	0	Full access.
01h	00000	0	0	1	Write locked. Default state at power-up.
02h	00000	0	1	0	Locked open (full access locked down).
03h	00000	0	1	1	Write-locked down.
04h	00000	1	0	0	Read locked.
05h	00000	1	0	1	Read and write locked.
06h	00000	1	1	0	Read-locked down.
07h	00000	1	1	1	Read-locked and write-locked down.

REGISTERS (CONTINUED)

Table 8. Pm49FL002 Block Locking Register Address

Register	Block Size (Kbytes)	Protected Block Address Range	Memory Map Address
T_BLOCK_LK	16	3C000h - 3FFFFh	FFBF8002h
T_MINUS01_LK	16 16 16	38000h - 3BFFFh 34000h - 37FFFh 30000h - 33FFFh	FFBF0002h
T_MINUS02_LK	16 16	2C000h - 2FFFFh 28000h - 2BFFFh	FFBE8002h
T_MINUS03_LK	16 16	24000h - 27FFFh 20000h - 23FFFh	FFBE0002h
T_MINUS04_LK	16 16	1C000h - 1FFFFh 18000h - 1BFFFh	FFBD8002h
T_MINUS05_LK	16 16	14000h - 17FFFh 10000h - 13FFFh	FFBD0002h
T_MINUS06_LK	16 16	0C000h - 0FFFFh 08000h - 0BFFFh	FFBC8002h
T_MINUS07_LK	16 16	04000h - 07FFFh 00000h - 03FFFh	FFBC0002h

Table 9. Pm49FL004 Block Locking Register Address

Register	Block Size (Kbytes)	Protected Block Address Range	Memory Map Address
T_BLOCK_LK	64	70000h - 7FFFFh	FFBF0002h
T_MINUS01_LK	64	60000h - 6FFFFh	FFBE0002h
T_MINUS02_LK	64	50000h - 5FFFFh	FFBD0002h
T_MINUS03_LK	64	40000h - 4FFFFh	FFBC0002h
T_MINUS04_LK	64	30000h - 3FFFFh	FFBB0002h
T_MINUS05_LK	64	20000h - 2FFFFh	FFBA0002h
T_MINUS06_LK	64	10000h - 1FFFFh	FFB90002h
T_MINUS07_LK	64	00000h - 0FFFFh	FFB80002h

A/A MUX MODE OPERATION

A/A MUX MODE READ/WRITE OPERATION

The Pm49FL002/004 offers a Address/Address Multiplexed (A/A Mux) mode for off-system operation, typically on an EPROM Programmer, similar to a traditional Flash memory except the address input is multiplexed. In the A/A Mux mode, the programmer must drive the OE# pin to low (V_{IL}) for read or WE# pins to low for write operation. The devices have no Chip Enable (CE#) pin for chip selection and activation as traditional Flash memory. The R/C#, OE# and WE# pins are used to activate the device and control the power. The 11 multiplex address pins - A[10:0] and a R/C# pin are used to load the row and column addresses for the target memory location. The row addresses (internal address A10 - A0) are latched on the falling edge of R/C# pin. The column addresses (internal address A21 - A11) are latched on the rising edge of R/C# pin. The Pm49FL002 uses A17 - A0 internally to decode and access the 256 Kbytes memory space. The Pm49FL004 use A18 - A0 respectively.

During a read operation, the OE# signal is used to control the output of data to the 8 I/O pins - I/O[7:0]. During a write operation, the WE# signal is used to latch the input data from I/O[7:0]. See Table 10 for Bus Operation Modes.

Table 10. A/A Mux Mode Bus Operation Modes

Mode	RST#	OE#	WE#	Address	I/O
Read	V_{IH}	V_{IL}	V_{IH}	X (1)	D_{OUT}
Write	V_{IH}	V_{IH}	V_{IL}	X	D_{IN}
Standby	V_{IH}	V_{IH}	V_{IH}	X	High Z
Output Disable	V_{IH}	V_{IH}	X	X	High Z
Reset	V_{IL}	X	X	X	High Z
Product Identification	V_{IH}	V_{IL}	V_{IH}	A2 - A21 = X, A1 = V_{IL}, A0 = V_{IL} and A1 = V_{IH}, A0 = V_{IH}	Manufacturer ID (2)
				A2 - A21 = X, A1 = V_{IL}, A0 = V_{IH}	Device ID (2)

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to Table 1 for the Manufacturer ID and Device ID of devices.

SYSTEM MEMORY MAP

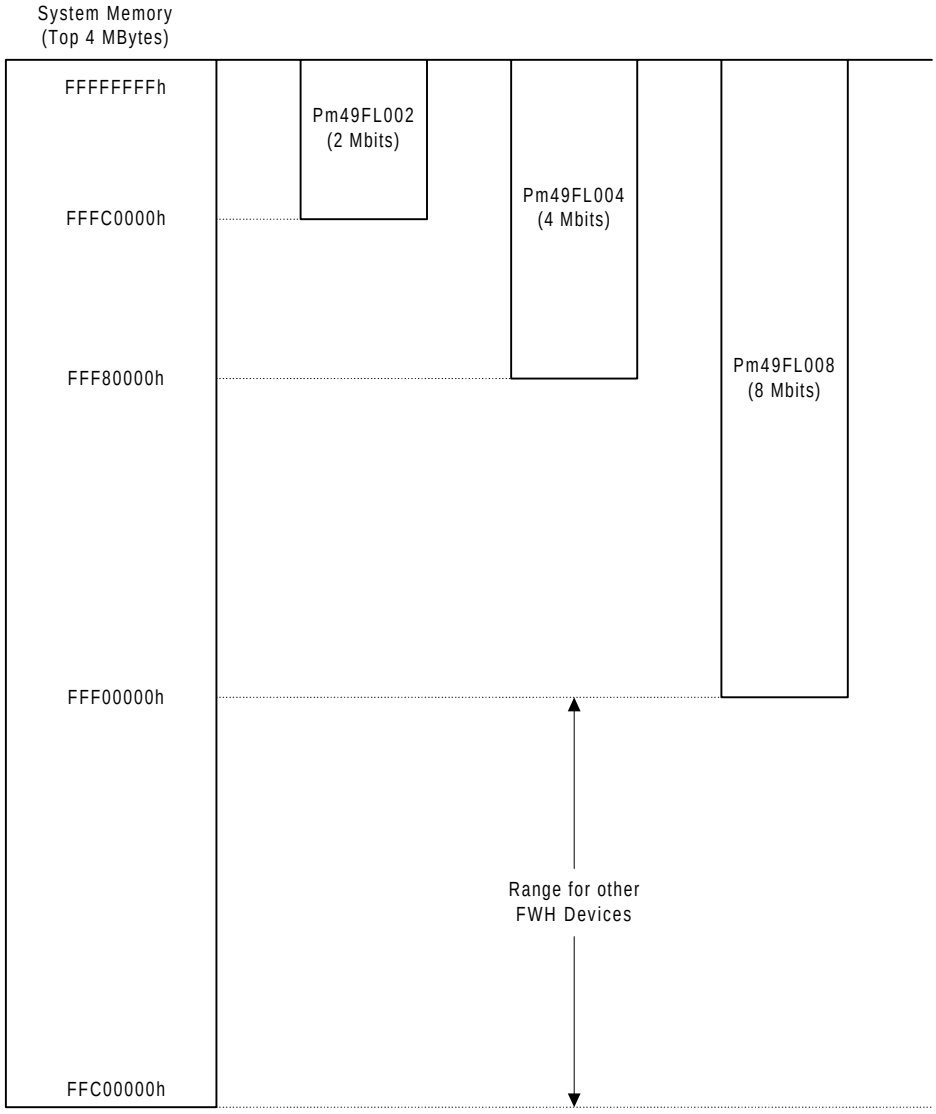


Table 11. System Memory Map

MEMORY BLOCKS AND ADDRESSES

Table 12. Pm49FL002 Sector/Block Address Table

Hardware Protection	Block	Block Size (Kbytes)	Sector	Sector Size (Kbytes)	Address Range
TBL#	Block 15 (Boot Block)	16	"	"	3C000h - 3FFFFh
WP#	Block 14	16	"	"	38000h - 3BFFFh
	Block 13	16	"	"	34000h - 37FFFh
	Block 12	16	"	"	30000h - 33FFFh
	Block 11	16	"	"	2C000h - 2FFFFh
	Block 10	16	"	"	28000h - 2BFFFh
	Block 9	16	"	"	24000h - 27FFFh
	Block 8	16	"	"	20000h - 23FFFh
	Block 7	16	"	"	1C000h - 1FFFFh
	Block 6	16	"	"	18000h - 1BFFFh
	Block 5	16	"	"	14000h - 17FFFh
	Block 4	16	"	"	10000h - 13FFFh
	Block 3	16	"	"	0C000h - 0FFFFh
	Block 2	16	"	"	08000h - 0BFFFh
	Block 1	16	"	"	04000h - 07FFFh
	Block 0	16	Sector 3	4	03000h - 03FFFh
			Sector 2	4	02000h - 02FFFh
			Sector 1	4	01000h - 01FFFh
			Sector 0	4	00000h - 00FFFh

MEMORY BLOCKS AND ADDRESSES (CONTINUED)

Table 13. Pm49FL004 Sector/Block Address Table

Hardware Protection	Block	Block Size (Kbytes)	Sector	Sector Size (Kbytes)	Address Range
TBL#	Block 7 (Boot Block)	64	"	"	70000h - 7FFFFh
WP#	Block 6	64	"	"	60000h - 6FFFFh
	Block 5	64	"	"	50000h - 5FFFFh
	Block 4	64	"	"	40000h - 4FFFFh
	Block 3	64	"	"	30000h - 3FFFFh
	Block 2	64	"	"	20000h - 2FFFFh
	Block 1	64	"	"	10000h - 1FFFFh
	Block 0	64	Sector 15	4	0F000h - 0FFFFh
			:	:	:
			Sector 1	4	01000h - 01FFFh
			Sector 0	4	00000h - 00FFFh

COMMAND DEFINITION

Table 14. Software Data Protection Command Definition

Command Sequence	Bus Cycle	1st Bus Cycle Addr[2] Data	2nd Bus Cycle Addr Data	3rd Bus Cycle Addr Data	4th Bus Cycle Addr Data	5th Bus Cylce Addr Data	6th Bus Cycle Addr Data
Read	1	Addr D_{OUT}					
Chip Erase [1]	6	5555h AAh	2AAAh 55h	5555h 80h	5555h AAh	2AAAh 55h	5555h 10h
Sector Erase	6	5555h AAh	2AAAh 55h	5555h 80h	5555h AAh	2AAAh 55h	SA [3] 30h
Block Erase	6	5555h AAh	2AAAh 55h	5555h 80h	5555h AAh	2AAAh 55h	BA [4] 50h
Byte Program	4	5555h AAh	2AAAh 55h	5555h A0h	Addr D_{IN}		
Product ID Entry	3	5555h AAh	2AAAh 55h	5555h 90h			
Product ID Exit [5]	3	5555h AAh	2AAAh 55h	5555h F0h			
Product ID Exit [5]	1	XXXXh F0h					

Notes:
1. Chip erase is available in A/A Mux Mode only.
2. Address A[15:0] is used for SDP command decoding internally and A15 must be “0” in FWH/LPC and A/A Mux modes. A_{MS} - A16 = Don’t care where A_{MS} is the most-significant address of Pm49FL00x.
3. SA = Sector address to be erased.
4. BA = Block address to be erased.
5. Either one of the Product ID Exit command can be used.

DEVICE OPERATIONS FLOWCHARTS

AUTOMATIC PROGRAMMING

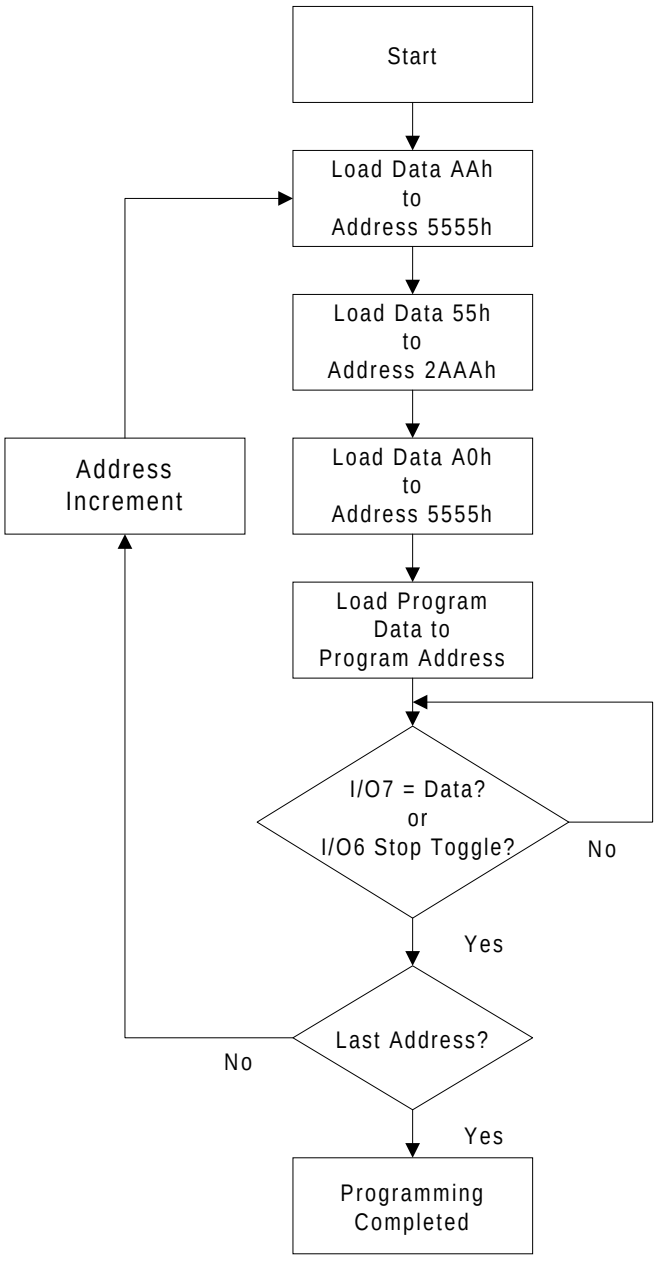
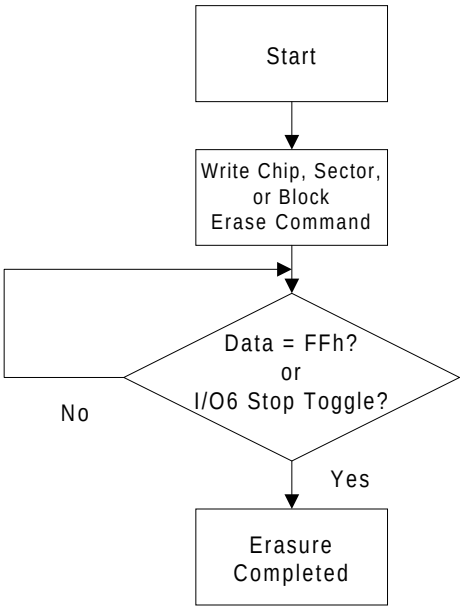


Chart 1. Automatic Programming Flowchart

DEVICE OPERATIONS FLOWCHARTS (CONTINUED)

AUTOMATIC ERASE



Notes:
1. Please see Table 12 to Table 13 for Sector/Block Address Tables.
2. Only erase one sector or one block per erase operation.
3. When the TBL# pin is pulled low (V_{IL}), the boot block will not be erased.

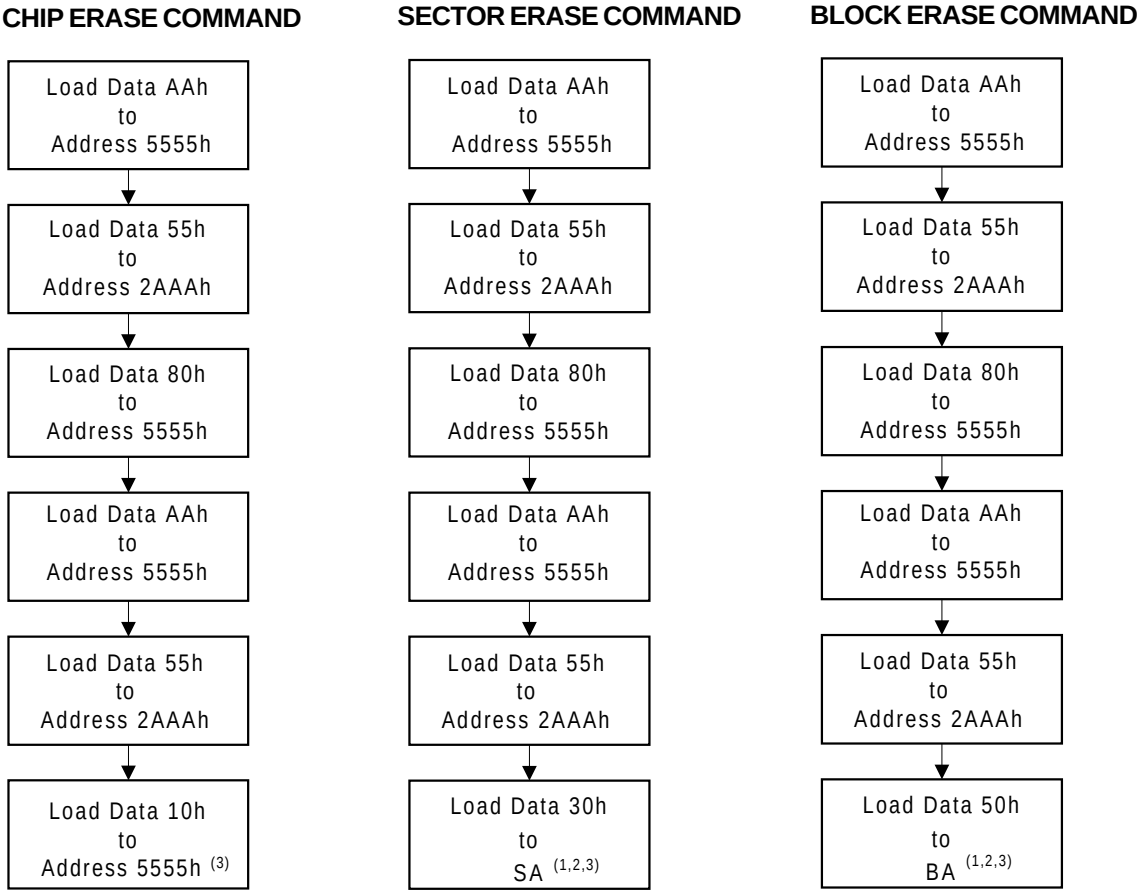
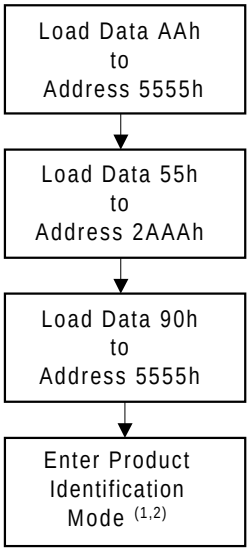


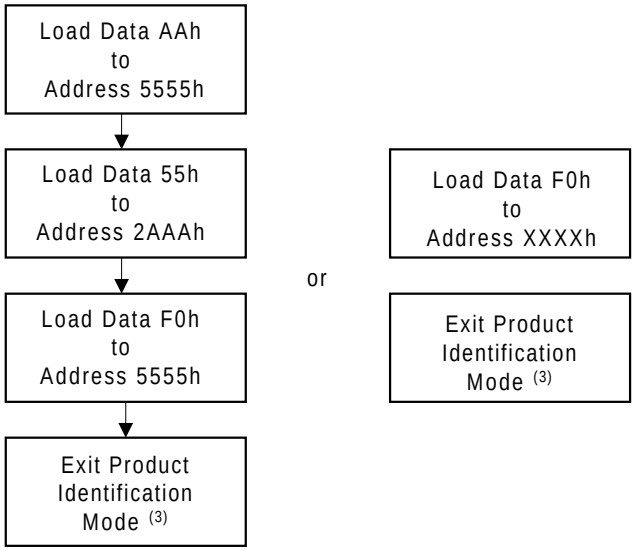
Chart 2. Automatic Erase Flowchart

DEVICE OPERATIONS FLOWCHARTS (CONTINUED)

SOFTWARE PRODUCT IDENTIFICATION ENTRY



SOFTWARE PRODUCT IDENTIFICATION EXIT



Notes:
1. After entering Product Identification Mode, the Manufacturer ID and the Device ID of Pm49FL00x can be read.
2. Product Identification Exit command is required to end the Product Identification mode and return to standby mode.
3. Either Product Identification Exit command can be used, the device returns to standby mode.

Chart 3. Software Product Identification Entry/Exit Flowchart

ABSOLUTE MAXIMUM RATINGS (1)

Temperature Under Bias		-55°C to +125°C
Storage Temperature		-65°C to +150°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins (2)		-0.5 V to V_{CC} + 0.5 V
All Output Voltage with Respect to Ground		-0.5 V to V_{CC} + 0.5 V
V_{CC} (2)		-0.5 V to +6.0 V

Notes:
1. Stresses under those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. The functional operation of the device or any other conditions under those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affected device reliability.
2. Maximum DC voltage on input or I/O pins are +6.25 V. During voltage transitioning period, input or I/O pins may overshoot to V_{CC} + 2.0 V for a period of time up to 20 ns. Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitioning period, input or I/O pins may undershoot GND to -2.0 V for a period of time up to 20 ns.

DC AND AC OPERATING RANGE

Part Number	**Pm49FL002**	**Pm49FL004**
Operating Temperature	0°C to 70°C	0°C to 70°C
Vcc Power Supply	3.0 V - 3.6 V	3.0 V - 3.6 V

DC CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_I	Input Leakage Current for IC, ID[3:0] pins	V_{IN} = 0 V to V_{CC}, V_{CC} = $V_{CC\,max}$			100	µA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}, V_{CC} = $V_{CC\,max}$			±1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}, V_{CC} = $V_{CC\,max}$			±1	µA
I_{SB}	Standby V_{CC} Current (FWH/LPC Mode)	FWH4 or LFRAME# = V_{IH}, f = 33 MHz; V_{CC} = $V_{CC\,max}$			500	µA
I_{RY}	Ready Mode V_{CC} Current (FWH/LPC Mode)	FWH4 or LFRAME# = V_{IL}, f = 33 MHz; I_{OUT} = 0 mA, V_{CC} = $V_{CC\,max}$			10	mA
I_{CC1}	V_{CC} Active Read Current (FWH/LPC Mode)	FWH4 or LFRAME# = V_{IL}, f = 33 MHz; I_{OUT} = 0 mA, V_{CC} = $V_{CC\,max}$		2	15	mA
I_{CC2} (1)	V_{CC} Program/Erase Current			7	20	mA
V_{IL}	Input Low Voltage		-0.5		0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA, V_{CC} = $V_{CC\,min}$			0.1 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA, V_{CC} = $V_{CC\,min}$	0.9 V_{CC}			V

Note: 1. Characterized but not 100% tested.

AC CHARACTERISTICS

PIN IMPEDANCE (V_{CC} = 3.3 V, f = 1 MHz, T = 25°C)

	Typ	Max	Units	Conditions
$C_{I/O}$ (1)	I/O Pin Capacitance	12	pF	$V_{I/O}$ = 0 V
C_{IN} (1)	Input Capacitance	12	pF	V_{IN} = 0 V
L_{PIN} (2)	Pin Inductance	20	nH	

Notes:
1. These parameters are characterized but not 100% tested.
2. Refer to PCI specification.

AC CHARACTERISTICS (CONTINUED)

FWH/LPC INTERFACE AC INPUT/OUTPUT CHARACTERISTICS

Symbol	Parameter	Condition	Min	Max	Units
I_{OH} (AC)	Switching current high	$0 < V_{OUT} < 0.3\ V_{CC}$	$-12\ V_{CC}$		mA
		$0.3\ V_{CC} < V_{OUT} < 0.9\ V_{CC}$	$-17.1\ (V_{CC} - V_{OUT})$		mA
		$0.7\ V_{CC} < V_{OUT} < V_{CC}$		Equation C (1)	
	(Test point)	$V_{OUT} = 0.7\ V_{CC}$		$-32\ V_{CC}$	mA
I_{OL} (AC)	Switching current low	$V_{CC} > V_{OUT} > 0.6\ V_{CC}$	$16\ V_{CC}$		mA
		$0.6\ V_{CC} > V_{OUT} > 0.1\ V_{CC}$	$-17.1\ (V_{CC} - V_{OUT})$		mA
		$0.18\ V_{CC} > V_{OUT} > 0$		Equation D (1)	
	(Test point)	$V_{OUT} = 0.18\ V_{CC}$		$38\ V_{CC}$	mA
I_{CL}	Low clamp current	$-3 < V_{IN} < -1$	$-25 + (V_{IN} + 1) / 0.015$		mA
I_{CH}	High clamp current	$V_{CC} + 4 > V_{IN} > V_{CC} + 1$	$25 + (V_{IN} - V_{CC} - 1) / 0.015$		mA
slewr (2)	Output rise slew rate	$0.2\ V_{CC}$ - $0.6\ V_{CC}$ load	1	4	V/ns
slewf (2)	Output fall slew rate	$0.6\ V_{CC}$ - $0.2\ V_{CC}$ load	1	4	V/ns

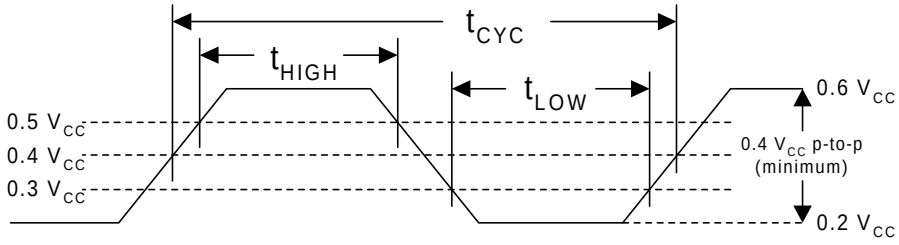
Notes:
1. See PCI specification.
2. PCI specification output load is used.

FWH/LPC INTERFACE CLOCK CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
t_{CYC}	Clock Cycle Time	30		ns
t_{HIGH}	Clock High Time	11		ns
t_{LOW}	Clock Low Time	11		ns
	Clock Slew Rate	1	4	V/ns
	lNIT# or RST# Slew Rate	50		mV/ns

AC CHARACTERISTICS (CONTINUED)

FWH/LPC INTERFACE CLOCK WAVEFORM



FWH/LPC INTERFACE MEASUREMENT CONDITION PARAMETERS

Symbol	Value	Units
V_{TH}[1]	0.6 V_{CC}	V
V_{TL}[1]	0.2 V_{CC}	V
V_{TEST}	0.4 V_{CC}	V
V_{MAX}[1]	0.4 V_{CC}	V
Input Signal Edge Rate	1 V/ns	

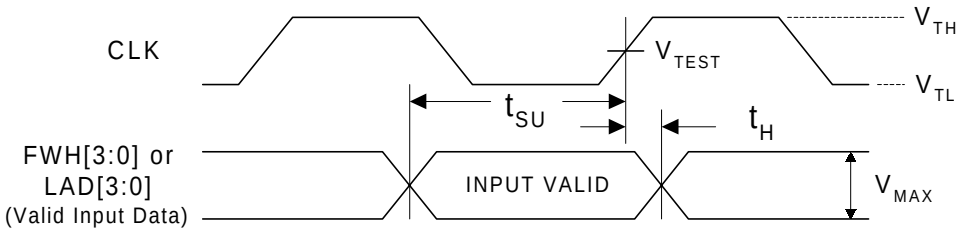
Note: 1. The input test environment is done with 0.1 V_{CC} of overdrive over V_{IH} and V_{IL}. Timing parameters must be met with no more overdrive that this. V_{MAX} specifies the maximum peak-to-peak waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameter.

FWH/LPC MEMORY READ/WRITE OPERATIONS CHARACTERISTICS

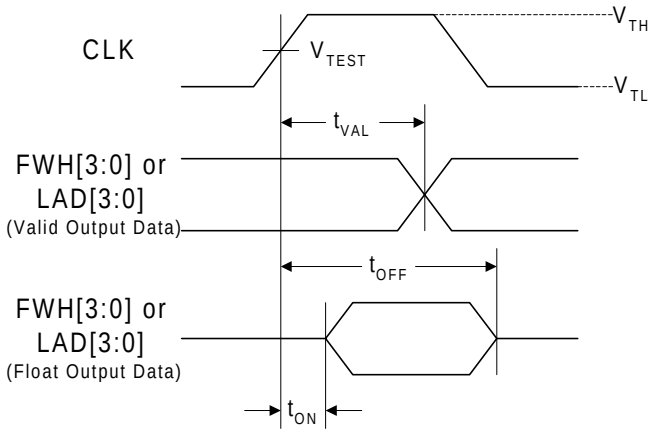
Symbol	Parameter	Min	Max	Units
T_{CYC}	Clock Cycle Time	30		ns
T_{SU}	Input Set Up Time	7		ns
T_{H}	Input Hold Time	0		ns
T_{VAL}	Clock to Data Out	2	11	ns
T_{ON}	Clock to Active Time (float to active delay)	2		ns
T_{OFF}	Clock to Inactive Time (active to float delay)		28	ns

AC CHARACTERISTICS (CONTINUED)

FWH/LPC INPUT TIMING PARAMETERS



FWH/LPC OUTPUT TIMING PARAMETERS



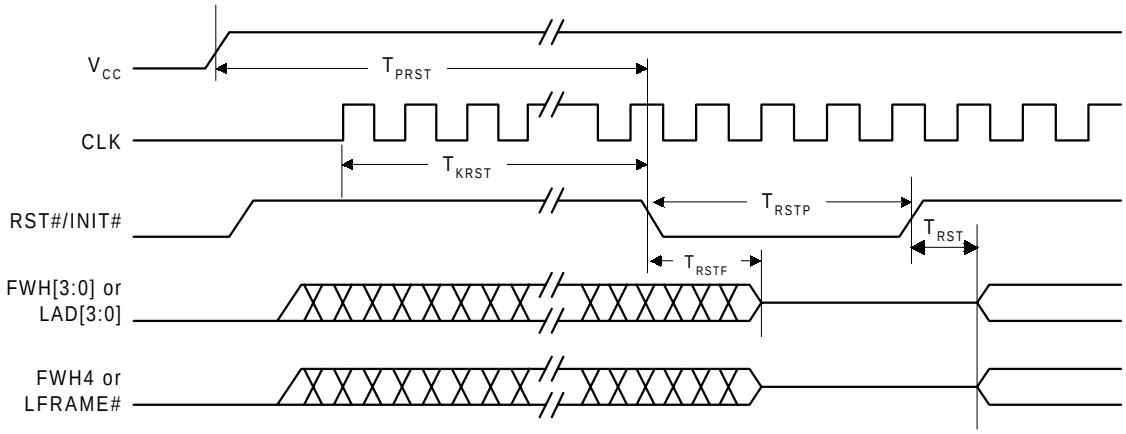
AC CHARACTERISTICS (CONTINUED)

FWH/LPC RESET OPERATION CHARACTERISTICS

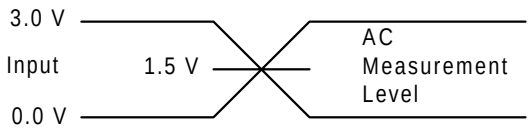
Symbol	Parameter	Min	Max	Units
T_{PRST}	Reset Active Time to V_{CC} Stable	1		ms
T_{KRST}	Reset Active Time to Clock Stable	100		µs
T_{RSTP}	Reset Pulse Width	100		ns
T_{RSTF}	Reset Active to Output Float Delay		50	ns
T_{RST} (1)	Reset Inactive Time to Input Active	1		µs

Note: 1. There will be a 10 µs reset latency if a reset procedure is performed during a programming or erase operation.

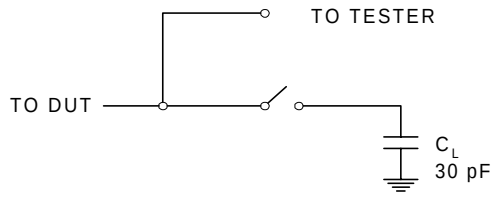
FWH/LPC RESET AC WAVEFORMS



A/A MUX MODE INPUT TEST MEASUREMENT CONDITION PARAMETERS



A/A MUX MODE TEST LOAD CONDITION

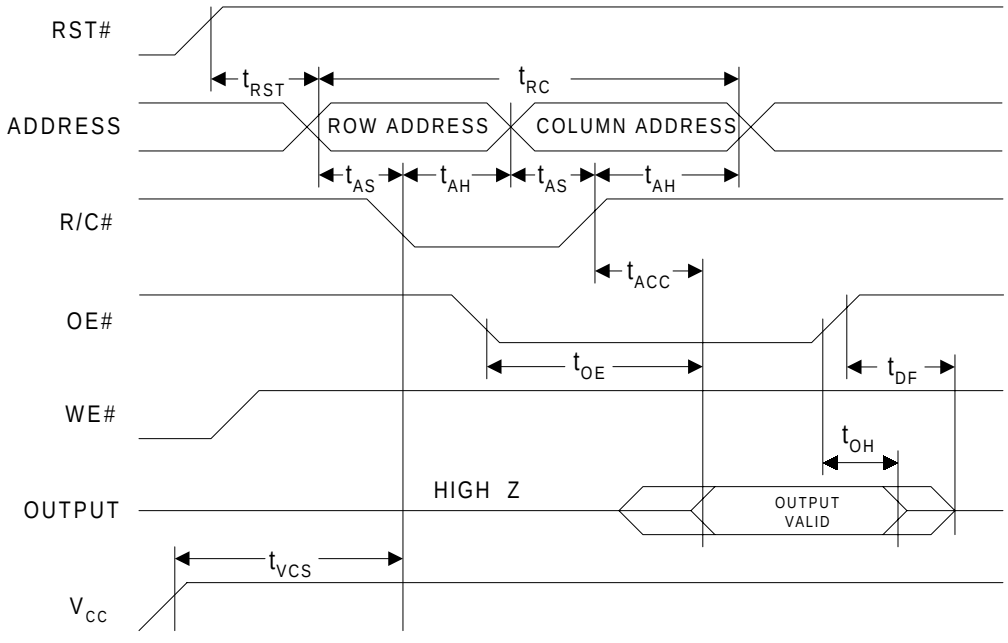


AC CHARACTERISTICS (CONTINUED)

A/A MUX MODE READ OPERATIONS CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
t_{RC}	Read Cycle Time	270		ns
t_{ACC}	Address to Output Delay		120	ns
t_{RST}	RST# High to Row Address Set-up Time	1		ms
t_{AS}	R/C# Address Set-up Time	45		ns
t_{AH}	R/C# Address Hold Time	45		ns
t_{OE}	OE# to Output Delay		50	ns
t_{DF}	OE# to Output High Z	0	30	ns
t_{OH}	Output Hold from OE# or Address, whichever occured first	0		ns
t_{VCS}	V_{CC} Set-up Time	50		µs

A/A MUX MODE READ OPERATIONS AC WAVEFORMS

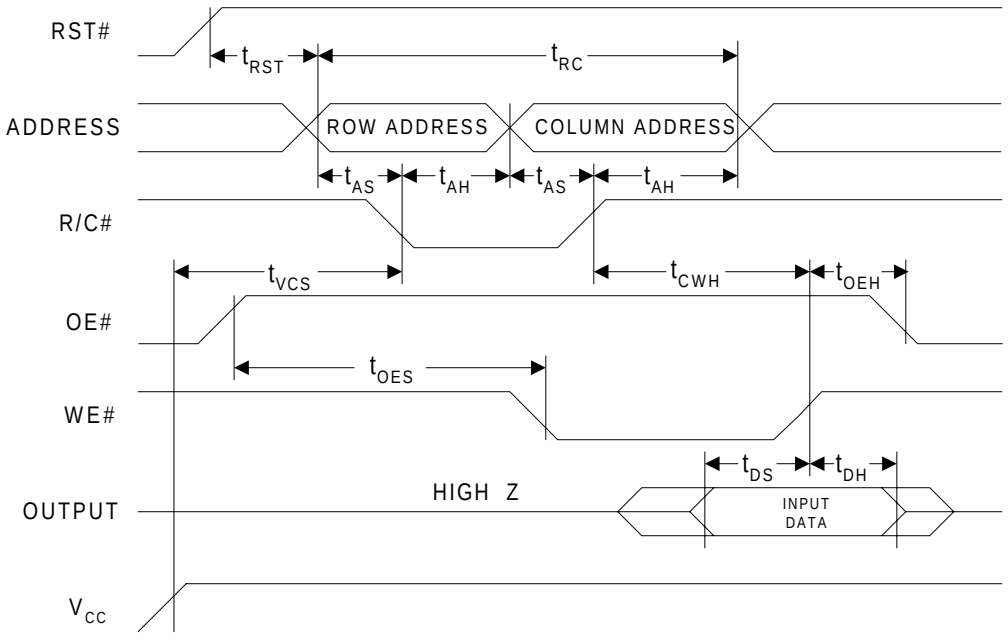


AC CHARACTERISTICS (CONTINUED)

A/A MUX MODE WRITE (PROGRAM/ERASE) OPERATIONS CHARACTERISTICS

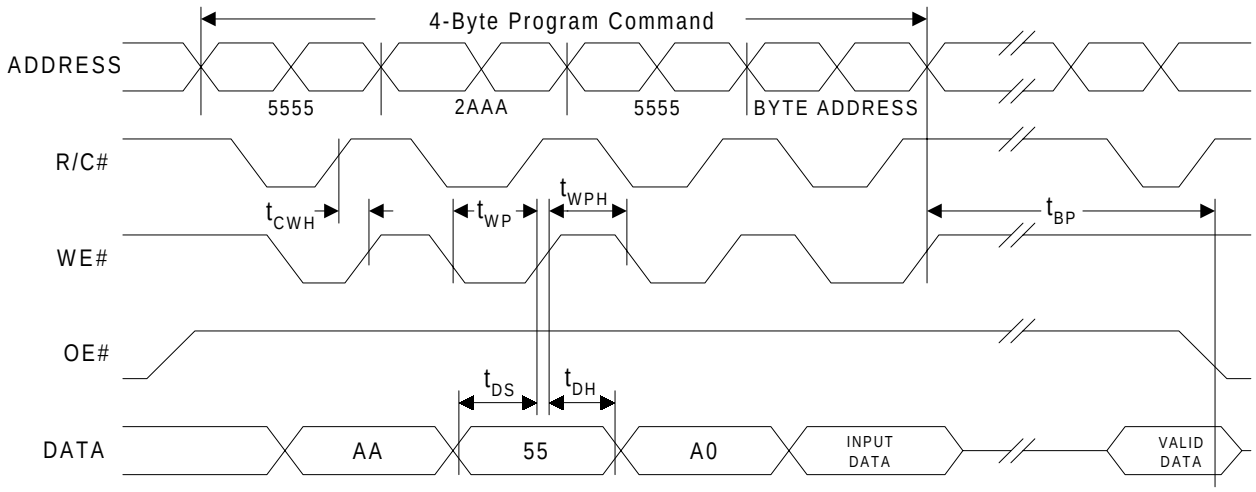
Symbol	Parameter	Min	Max	Units
t_{RST}	RST# High to Row Address Set-up Time	1		ms
t_{AS}	R/C# Address Set-up Time	50		ns
t_{AH}	R/C# Address Hold Time	50		ns
t_{CWH}	R/C# to WE# High Time	50		ns
t_{OES}	OE# High Set-up Time	20		ns
t_{OEH}	OE# High Hold Time	20		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	5		ns
t_{WP}	Write Pulse Width	100		ns
t_{WPH}	Write Pulse Width High	100		ns
t_{BP}	Byte Programming Time		40	µs
t_{EC}	Chip, Sector or Block Erase Cycle Time		80	ms
t_{VCS}	V_{CC} Set-up Time	50		µs

A/A MUX MODE WRITE OPERATIONS AC WAVEFORMS

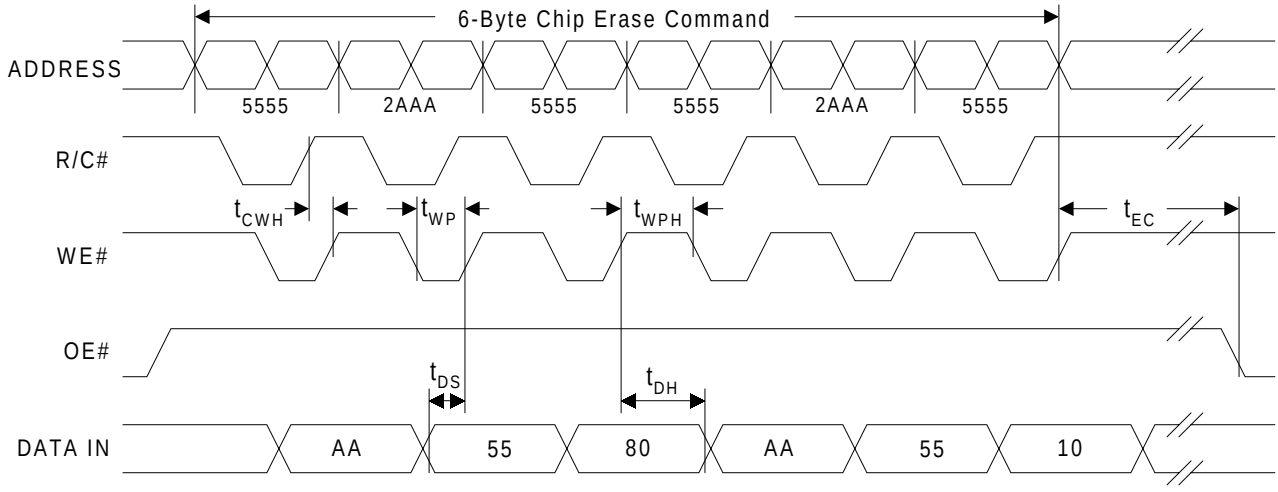


AC CHARACTERISTICS (CONTINUED)

A/A MUX MODE BYTE PROGRAM OPERATIONS AC WAVEFORMS

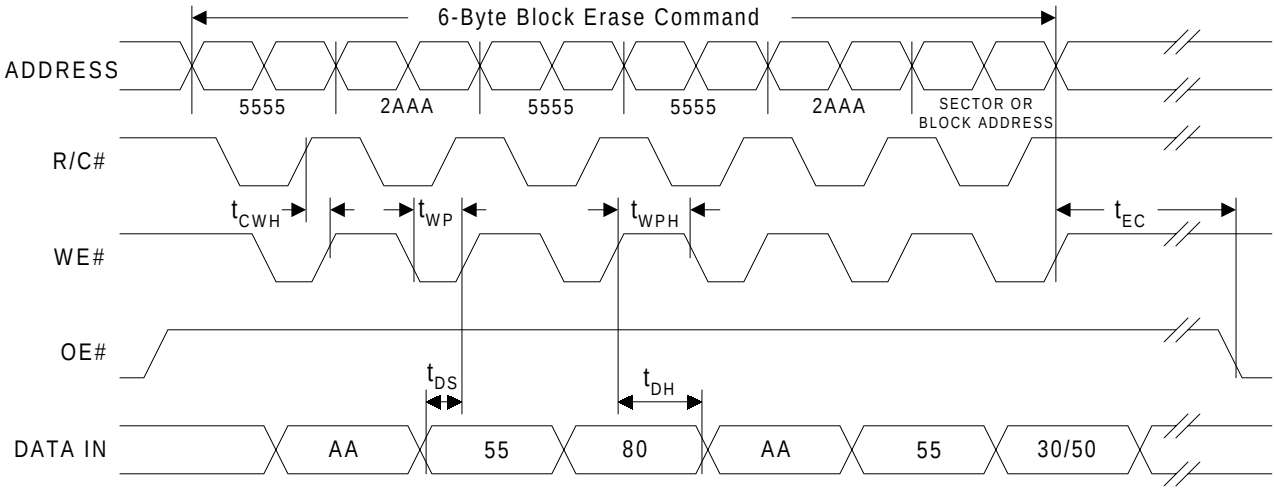


A/A MUX MODE CHIP ERASE OPERATIONS AC WAVEFORMS

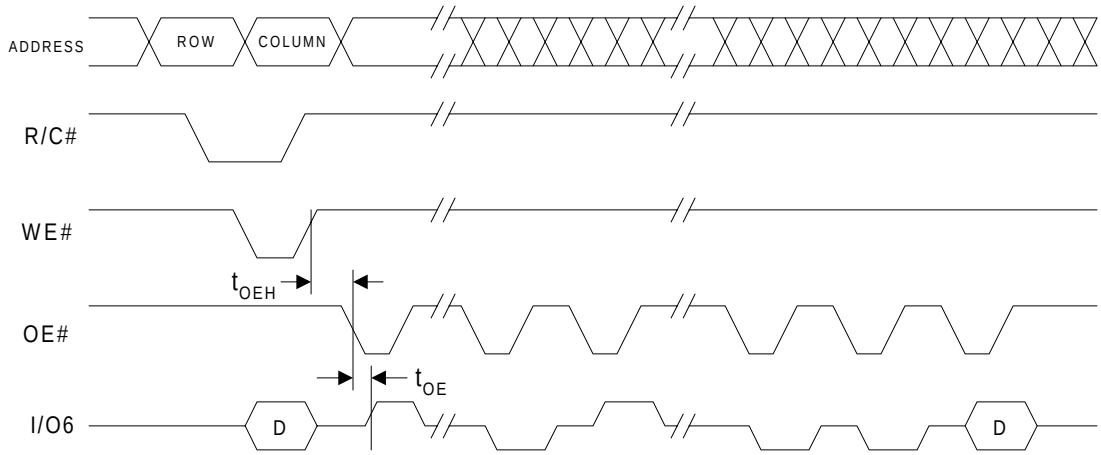


AC CHARACTERISTICS (CONTINUED)

A/A MUX MODE SECTOR/BLOCK ERASE OPERATIONS AC WAVEFORMS



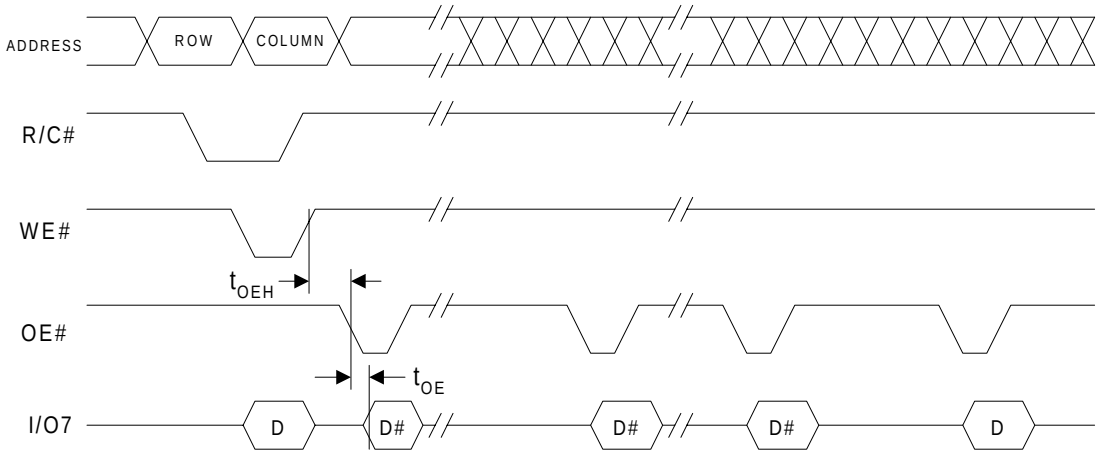
A/A MUX MODE TOGGLE BIT AC WAVEFORMS



Note: 1. Toggling OE# will operate Toggle Bit.
2. I/O6 may start and end from “1” or “0” in random.

AC CHARACTERISTICS (CONTINUED)

A/A MUX MODE DATA# POLLING AC WAVEFORMS



Note: Toggling OE# will operate Data# Polling.

PROGRAM/ERASE PERFORMANCE

Parameter	Unit	Typ	Max	Remarks
Sector/Block Erase Time	ms	50	80	From writing erase command to erase completion
Chip Erase Time	ms	50	80	From writing erase command to erase completion
Byte Programming Time	µs	25	40	Excludes the time of four-cycle program command execution

Note: These parameters are characterized but not 100% tested.

RELIABILITY CHARACTERISTICS (1)

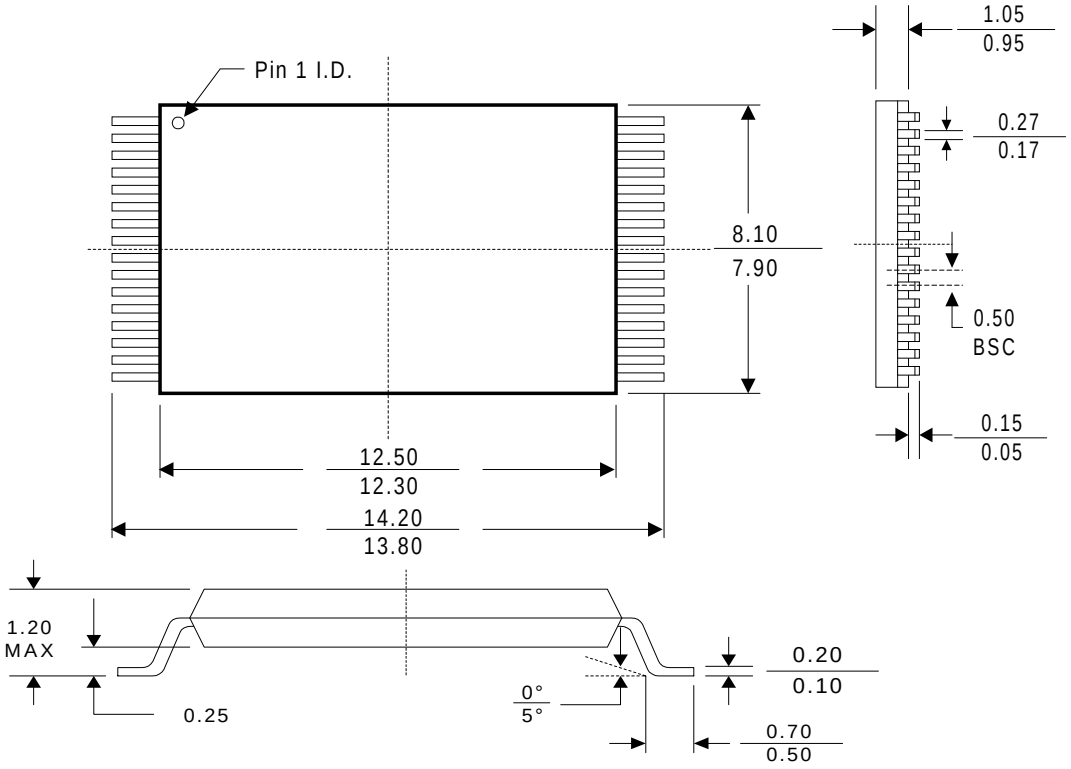
Parameter	Min	Typ	Unit	Test Method
Endurance	100,000 (2)		Cycles	JEDEC Standard A117
Data Retention	20		Years	JEDEC Standard A103
ESD - Human Body Model	2,000	>4,000	Volts	JEDEC Standard A114
ESD - Machine Model	200	>400	Volts	JEDEC Standard A115
Latch-Up	100 + I_{CC1}		mA	JEDEC Standard 78

Notes: 1. These parameters are characterized but not 100% tested.
2. Preliminary specification only and will be formalized after cycling qualification test.

PACKAGE TYPE INFORMATION

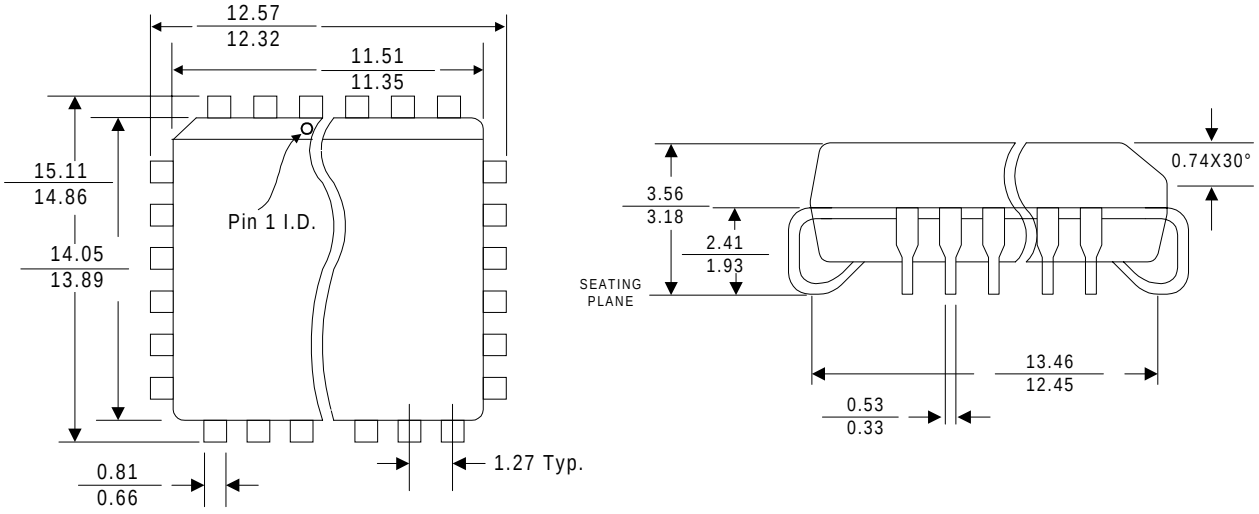
32V

32-Pin Thin Small Outline Package (VSOP - 8 mm x 14 mm)(measure in millimeters)



32J

32-Pin Plastic Leaded Chip Carrier (measured in millimeters)



TOP VIEW **SIDE VIEW**

REVISION HISTORY

Date	Revision No.	Description of Changes	Page No.
June, 2002	1.0	Preliminary publication	All
July, 2002	1.1	Formal publication	All
January, 2003	1.2	Revised program and erase time specification	1, 41, 44
		Corrected typo on the part number for Block Locking Register	23
November, 2003	1.3	Removed Pm49FL008 information	All
		Removed inch measurement for package type information	45
December, 2003	1.4	Changed product ordering information for lead-free package option	1, 4, 34
		Upgraded guranteed program/erase cycles from 50,000 to 100,000 (preliminary)	1, 44